5.7 Power Transistor Reliability

5.7.1 Overview

(1) Features

Power transistors are, literally, devices for handling power. In general, this includes any transistor whose allowable collector dissipation Pc is greater than 1 watt. However, the characteristics and packages of power transistors vary greatly accotding to the application.

Typically, power transistors are classified by application (switching or audio) or by package (molded or canister). In recent years, the molded package has become prevalent because of its price competitiveness and improved reliability. There are also a few products which are supplied in a composite module package.

Power transistors of up to Pc = 300 W are available. Since power transistors are at the heart of application equipment, they must be highly reliable.

(2) Chip structures

Power transistors are fabricated with a chip structure appropriate for the intended application. The various chip structures used in power transistors are listed in Table 5.7.1.

Table 5.7.1 Power transistor chip structures

Transistor Type		Features	Application	Structure
Mesa		High withstand voltage Wide SOA	Large current-switching capacity Low-frequency power amplification	Figure 5.7.1
Planar	Epitaxial	Low saturation voltage Good h_{FE} linearity	High-speed switching High-frequency power amplification	Figure 5.7.2
	Triple-diffused	Wide SOA Low price	Low-frequency power amplification	Figure 5.7.2 (Note)

Note: Epitaxial wafer is used.

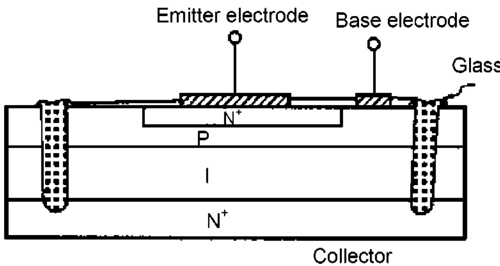


Figure 5.7.1 Glass mesa structure

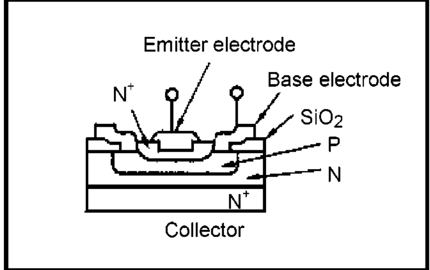


Figure 5.7.2 Epitaxial planar structure

(3) Internal structure

Power transistors normally have a source, gate and drain as internal chip electrodes. Generally, the collector is mounted on a frame that extends directly from the underside of the chip to serve as an external lead, while the emitter and base are connected to their respective leads with bonding wires.

A molded package transistor whose collector and heat sink are isolated from each other (referred to as an "isolated" transistor) has its frame coated with resin to an overall, even thickness of several hundred μm. This structure ensures that the specified isolation voltage is met and at the same time offers low thermal resistance. In addition, when a heat sink is not used, the high thermal conductivity of the resin provides better collector dissipation than conventional products.

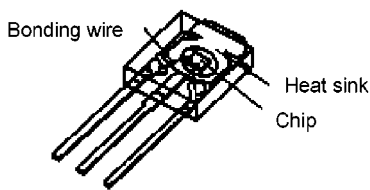


Figure 5.7.3 Molded package type

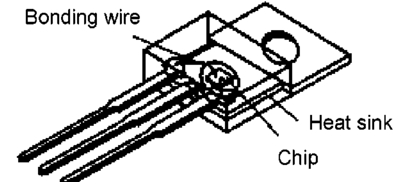


Figure 5.7.4 TO-220 (AB) package type

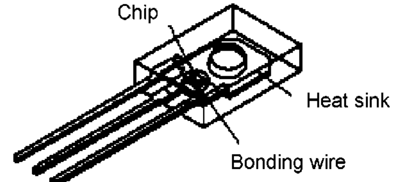


Figure 5.7.5 TO-126 (IS) package type

5.7.2 Usage Precautions

(1) Absolute maximum ratings

Transistor absolute maximum ratings are stipulated for three parameters: voltage, current and temperature. For power transistors, however, there are other equally, if not more, important parameters that must be considered, as described below.

(a) Safe operating area

The operating range within which transistors can be used safely without fear of breakdown or degradation is referred to as the safe operating area (SOA).

The operating range of transistors is normally limited by their maximum ratings, including the maximum voltage, maximum current and maximum collector dissipation. Power transistors used in large amplifiers or circuits with inductive loads, however, can degrade or break down even if operated within their absolute maximum ratings. This is attributable to a transistor phenomenon known as secondary breakdown.

The discovery of the secondary breakdown phenomenon in 1958 by C. G. Thornton, C. D. Simmons, et al gave rise to the concept of the safe operating area (SOA) as a means, along with the absolute maximum ratings, of regulating the operating range of transistors. An understanding of this concept is essential for designing economical, yet highly reliable, transistor circuits.

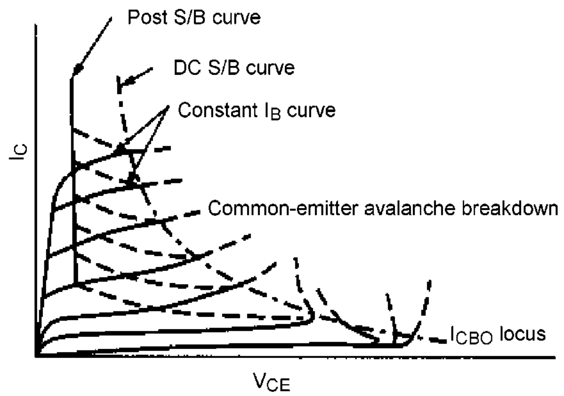
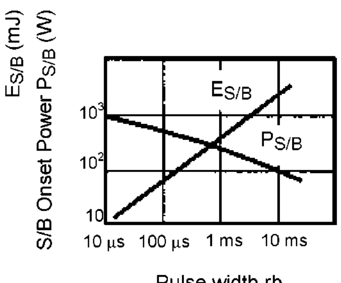


Figure 5.7.6 Collector output characteristics and S/B curves

1) Secondary Breakdown

The secondary breakdown (S/B) phenomenon occurs when certain voltage-current points ($V_{S/B}$, $I_{S/B}$) are reached (as the current continues to increase after a primary breakdown) and the collector-to-emitter voltage drops rapidly. This causes a transition into the low-impedance region (within several μs or less) as shown in Figure 5.7.6, often resulting in a breakdown of the transistor.
This phenomenon is observed regardless of whether the base-to-emitter is forward- or reverse-biased, and can occur with either V_{CEO} or V_{CBO}. However, the S/B onset points ($V_{S/B}$, $I_{S/B}$) do vary with base bias conditions and line up along the locus of the S/B curve as shown in Figure 5.7.6. Although the diagram shows the S/B phenomenon for a DC case, because the S/B onset characteristic is highly energy-dependent, the S/B curve varies with the applied pulse width.



The S/B curve defines the SOA with respect to the pulse. F shows the relationship between the pulse width of the applied power and the S/B. As the pulse width becomes narrow, the secondary breakdown energy (called triggering energy, referring to the energy that is absorbed by the transistor until S/B is reached) decreases, and the S/B power tolerance increases.

Figure 5.7.7 Pulse width vs. $E_{S/B}$ and $P_{S/B}$

Although many possible causes have been suggested for the S/B phenomenon, most people agree today on a theory which holds that a high-temperature area (called a "hot spot") is generated by a local concentration of current. This hot spot gives rise to what is known as "local thermal runaway". The current concentration is said to be caused by a voltage drop in the base area or an unstable temperature distribution in a lateral direction.

Current concentration can also be triggered by an uneven base width, a junction defect, or uneven fitting of the chip to the heat sink.

(b) Forward-bias S/B

When the base-to-emitter interval is forward-biased, a hot spot due to local current concentration is generated in the emitter periphery.

This is because the base current flowing immediately below the emitter in the lateral direction causes a voltage drop in the base area such that the emitter outer-edge sections are biased more than the emitter's central center section. For this reason, minority carrier injection into the base occurs mostly in the emitter periphery, and current density increases as shown in Figure 5.7.8 (a) and (b). Carriers crossing the collector depletion layer cause the power dissipation to increase and thus cause local heating. This, in turn, causes further current concentration. A vicious circle is thus entered, leading eventually to the generation of a hot spot and subsequent secondary breakdown.

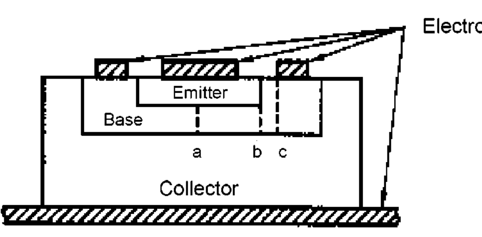


Figure 5.7.8 (a) Planar transistor

+ V_{BE}

Bias level

V_d

a b c

Figure 5.7.8 (b) Emitter forward bias

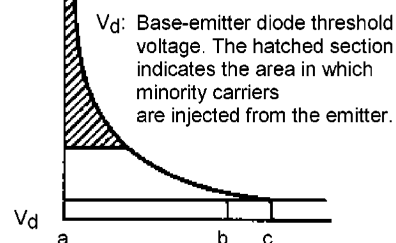
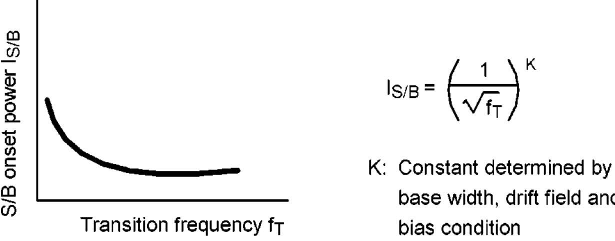


Figure 5.7.8 (c) Emitter reverse bias

The relationship between S/B and transistor characteristics

Current $I_{S/B}$ at the S/B onset point of a forward-biased transistor is closely related to the transistors' characteristics. When carriers injected from the emitter to the base area reach the collector junction, they generally fan out into a cone-shaped pattern. If the carriers take a long time to traverse the base area (this is known as the transit time), current density will have decreased by the time the carriers reach the collector depletion layer, making it less likely for a hot spot to occur. Since the carrier transit time is determined by the base width and the drift field in the base area, $I_{S/B}$ exhibits a strong correlation with the transistor frequency characteristic. Thus, f_T and $I_{S/B}$ have a negative correlation irrespective of the pulse width, as shown in Figure 5.7.9.



$$I_{S/B} = \left(\frac{1}{\sqrt{f_T}}\right)^K$$

K: Constant determined by base width, drift field and bias condition

Figure 5.7.9 Relationship between $I_{S/B}$ and f_T

(c) Reverse-bias S/B

When the base-to-emitter interval is reverse-biased, the voltage drop in the base area is in a direction opposite to that of the forward-biased case.

For this reason, carriers injected from the emitter concentrate in the center section of the emitter as shown in Figure 5.7.8 (c). (This carrier concentration varies according to transistor type. For ring-shaped emitters, it occurs at a single spot at the center of the emitter; for comb-shaped emitters, it occurs along a line at the center of the emitter.)

The greater the reverse bias, the more the carriers tend to concentrate in a very small centeral area. Accordingly, the triggering energy of a reverse-biased transistor (the energy absorbed by the transistor up until S/B occurs) is much smaller than that of a forward-biased transistor. Since the carriers injected from the emitter fan out as they propagate (as described above for the forward-biased case), the base width and the presence of a drift field in the base area have a strong correlation with S/B.

Reverse-biased S/B occurs mainly when there is an inductive load. The triggering energy $F_{S/B}$ depends on the inductance L and on the base-emitter conditions, as shown in Figure 5.7.10.

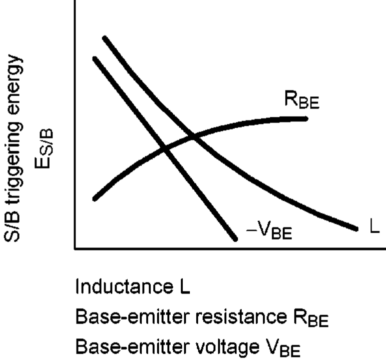


Figure 5.7.10 Dependency of S/B triggering energy $E_{S/B}$ upon load inductance and base-emitter conditions

(d) S/B phenomenon and transistor destruction/degradation

When S/B occurs, its effects on the transistor's electrical characteristics vary according to the type of the transistor. If the applied power is small, or the current is shut off the moment S/B occurs, the changes in electrical characteristics will be slight, or degradation will be gradual, even if S/B occurs repeatedly. In other cases, however, the transistor can break down after even a single occurrence of S/B.

A general symptom that can be observed in the electrical characteristics of transistors degraded or destroyed by S/B is a softening in the waveform, or a complete shorting out of V_{EBO}, V_{CBO} or V_{CEO}. In particular, a short between the emitter and collector is a typical symptom degradation caused by S/B, often associated with a hole melting from emitter to collector. In other cases, S/B tolerance can be reduced, even while other electrical characteristics appear normal, when the S/B triggering energy $E_{S/B}$ becomes small, causing the transistor to become more susceptible to breakdown.

(e) Reverse-bias SOA

Reverse-bias SOA cannot be determined as easily as forward-bias SOA. In L-load switching circuits, TV horizontal deflection output circuits and DC-DC converters, however, the base-emitter junction is often subjected to high voltages while it is reverse-biased. Therefore, the reverse-bias SOA is an important consideration in these circuits.

Figure 5.7.11 (a) shows the I_C-L characteristic of a transistor under certain reverse-bias conditions. Figure 5.7.11(b) and (c) show the derating of I_C for changes in V_{BB2} and R_{BB2} respectively. In simple L-load circuits, the SOA can be obtained directly from Figure 5.7.11. For more complex circuits, however, the effective value of L must first be determined before Figure 5.7.11 is consulted.

Normally, it is very difficult to find a generally applicable SOA like the one shown in Figure 5.7.11. For users too it is difficult to determine the SOA by obtaining the effective L from actual circuits and then using the diagrams. For this reason, Toshiba specify the SOA for its products in terms of I_C, V_{BB2} and R_{BB2} according to the products' intended use of the transistor and reject devices whose load characteristics do not conform to Figure 5.7.12 or which exhibit oscillation or flickering in the load curve.

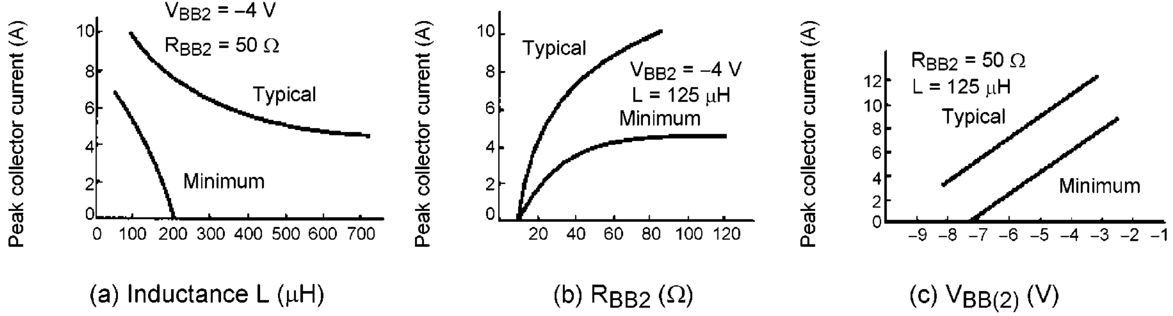


Figure 5.7.11 Examples of reverse-bias SOA

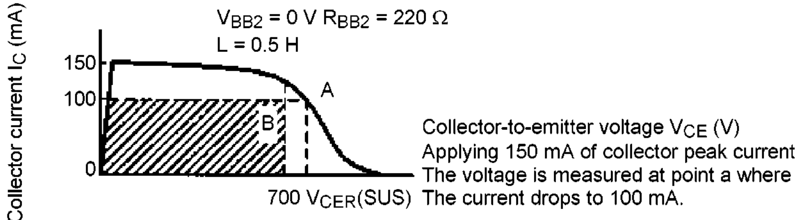


Figure 5.7.12 Example of reverse-bias SOA

(f) Maximum fastening torque

When using power transistors with a heat sink, take care not to apply excessive torque when tightening screws, to avoid cracking the plastic case or the transistor chip itself.

Table 5.7.2 lists recommended screw-tightening torques for each package type.

Table 5.7.2

Package		Screw-Tightening Torque (max)
JEDEC	Toshiba Name	
TO-220AB	2-10A1A	0.6 N•m
TO-220 (IS)	2-10L1A	0.6 N•m
TO-126 (IS)	2-8H1A	0.4 N•m
TO-3P	2-16B1A, C1A	0.8 N•m
TO-3P (NIS)	2-16F1A	0.6 N•m
T0-3P (L)	2-21F1A	0.8 N•m
TO-3P (H) (BS)	2-16D2A	0.8 N•m
TO-3P (H) (IS)	2-16E2A	0.6 N•m

(g) Derating

Since power transistors handle large amounts of power, power loss within the device due to operating conditions or circuit design can cause the junction temperature T_j to increase, narrowing the safe operating area (SOA). When designing circuits that use power transistors, you must derate the maximum values as shown below. Figure 5.7.13 shows some sample derating curves.

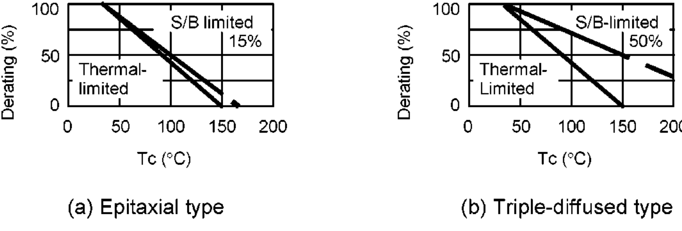


Figure 5.7.13 Temperature deratings for SOA

Note: The above diagram shows examples of SOA temperature derating in the thermal-limited and S/B-limited areas for epitaxial and triple-diffused structure transistors respectively.

(2) Applying usage precautions

- Attaching a heat sink

A heat sink is required for power transistors when the supply voltage, current load or ambient temperature is such that heat radiation is required. When using a heat sink, the following precautions must be observed to obtain sufficient heat radiation and to avoid applying stress to the transistor.

(a) Applying silicone grease

Apply a coating of silicone grease between the heat sink and the transistor to improve heat conductivity. Be sure to apply the coating thinly and evenly; do not use too much. Also, be sure to use a non-volatile grease, as volatile greases can crack over time, lessening the heat radiation capability.

If the transistor is housed in a plastic package, the fype of silicone grease to be applied between the heat sink and the device must be selected carefully. With some types of greases, the base oil separates and penetrates the plastic package, significantly reducing the useful life of the device.

Two recommended silicone greases in which base oil separation is not a problem are YG6260 from Toshiba Silicone and G746 from Shinetsu Chemical Ind.

The above precautions do not apply to metal-sealed transistors.

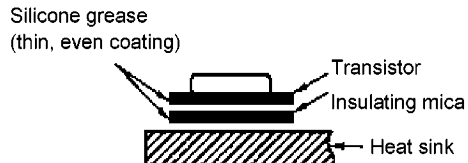
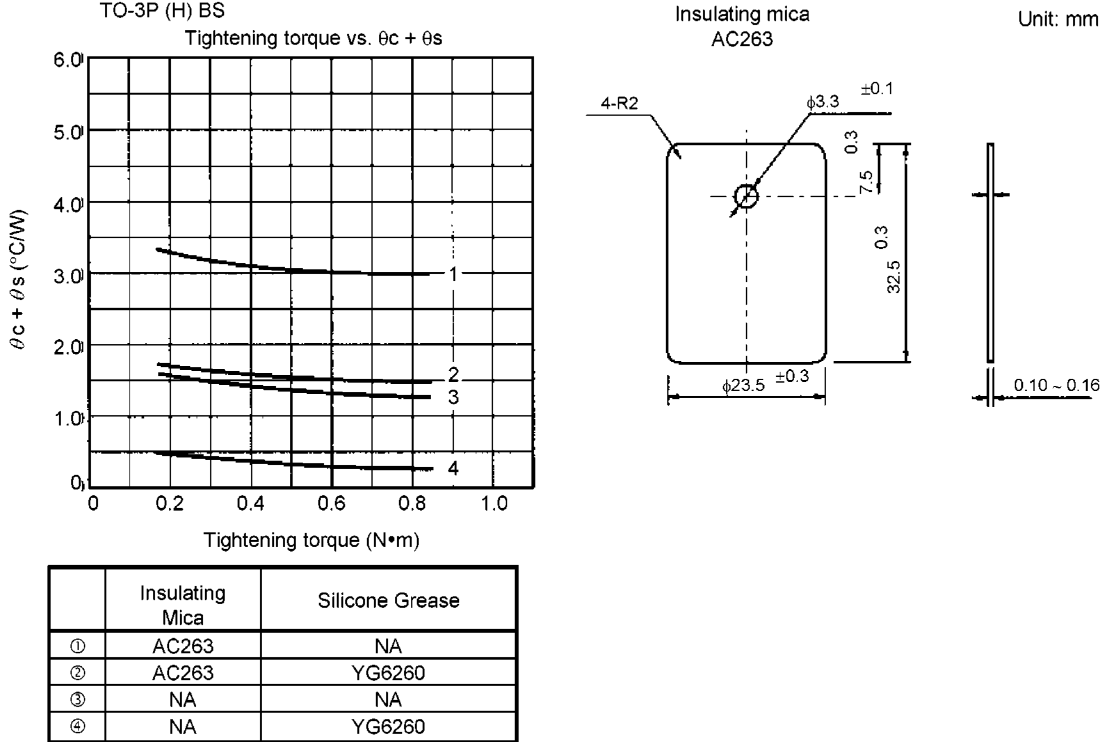


Figure 5.7.14 Applying a coating of silicone grease

(b) Fastening screws

Do not fasten screws with forces greater than the maximum fastening torque listed in Table 5.7.2. Excessive tightening can damage the device.

Figure 5.7.15 shows how thermal resistance becomes sufficiently saturated at a certain tightening torque.



	Insulating Mica	Silicone Grease
①	AC263	NA
②	AC263	YG6260
③	NA	NA
④	NA	YG6260

Figure 5.7.15

(c) Heat sink screws and screw hole diameters

When mounting power transistors on a circuit board, use the recommended mounting method and screws.

Do not use flush head screws as they subject the device to abnormal stresses. When using tapping screws, be careful of the debris that gets generated and make sure that the screw holes diameters of the in the heat sink are not too large.

(d) Clamping with a band

When clamping one or more power transistors with a band, as shown in Figure 5.7.16, remember that the metal fixture applies pressure to the mold package. In some cases, the resulting mechanical stress can cause the device to break down.

Note also that with isolated transistor types, the dielectric strength of the upper surface of the mold (the marked surface) is not guaranteed. Hence the transistor may not be properly insulated from the heat sink.

When considering the band clamp method for attaching power transistors to a circuit board, please consult first with the Toshiba Engineering Division.

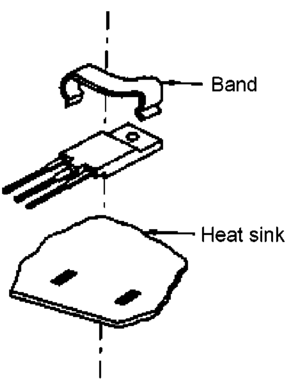


Figure 5.7.16

- Destruction

  Power transistors are often used in applications where the capacity on the power supply side is large and the impedance (load) between the power transistor and power supply is very low.

  If a power transistor fails for some reason under these conditions, it can explode, generating a loud noise and possibly producing smoke or fumes.

  When safety problems or other problems are anticipated, consider installing a protective unit and an appropriate fuse.

5.7.3 Reliability Characteristics

(1) Reliability test results

As an example, Table 5.7.3 lists the results of reliability tests conducted for a plastic-encapsulated low-frequency power amplification transistor. Table 5.7.3 lists the failure criteria applied during the test.

A basic method frequently used to evaluate reliability is to have a device in operation and to perform a detailed analysis of the changes that occur in its characteristics over time. As an example, Figure 5.7.17 to 5.7.19 show changes in characteristics that occurred during the lifetime test described in Table 5.7.3.

Test results indicate that, alchough the debice was perated as its absolute maximum ratings, the initial characteristics remained stable over a long period of time. Consequently, this device can be expected to offer high reliability in an application.

Table 5.7.3 Reliability test results for 2SD1406 low-frequency power amplification transistor

	Test Item	Applicable Standard JIS C7021	Test Conditions	No. Of Device Tested	No. Of Device Failures
Lifetime Tests	Steady-state operation	B-4	Pc = 2 W, Ta = 25°C, 1,000 hrs	30	0
	High-temperature reverse bias	B-8	Ta = 150°C, V_{CB} = 48 V 1,000 hrs	30	0
	High-temperature storage	B-10	Ta = 150°C, 1,000 hrs	30	0
	High-temperature, high-humidity storage	B-11	Ta = 60°C, RH = 90% 1,000 hrs	30	0
Environment Tests	Soldering heat	A-1	260°C, 10 secs, once (immersed 1.5 mm from base of device)	32	0
	Temperature cycling	A-4	−55°C to 25°C to 150°C to 25°C 100 cycles	50	0
	Thermal shock	A-3	100°C to 0°C, 50 cycles	32	0
	Moisture resistance	A-5	Ta = to 65°C, RH to 90% to 98% 10 cycles	32	0
Mechanical Tests	Vibration	A-10	100 Hz to 2,000 Hz, 196 m/s^2 (20 g) 4 times each in 3 directions	11	0
	Mechanical shock	A-7	14,700 m/s^2 (1,500 g), 0.5 ms 3 times each in 4 directions	11	0
	Constant acceleration	A-9	196,000 m/s^2 (20,000 g) 1 minute each in 6 directions	11	0
	Lead integrity	A-11	500 g, bent 90° 3 times	11	0
	Dropping	A-8	75 cm, on maple board, 3 times	11	0
	Solderability	A-2	230°C, 5 secs (using designated flux)	11	0

Table 2.7.3 Failure Criteria for 2SD1406

Parameter	Symbol	Measuring Conditions (Ta = 25°C)	Criteria		Remarks
			minimum	maximum	
Collector cut-off current	I_{CBO}	V_{CB} = 60 V, I_E = 0	—	200 μA	USL × 2
Emitter cut-off current	I_{EBO}	V_{EB} = 7 V, I_C = 0	—	200 μA	USL × 2
DC current amplification rate	h_{FE}	V_{CE} = 5 V, I_C = 0.5 A	48	360	USL × 1.2 LSL × 0.8
Collector-to-emitter breakdown voltage	V_{CEO}	I_C = 50 mA, I_B = 0	54 V	—	LSL × 0.9

USL: Upper specification limit; LSL: Lower specification limit

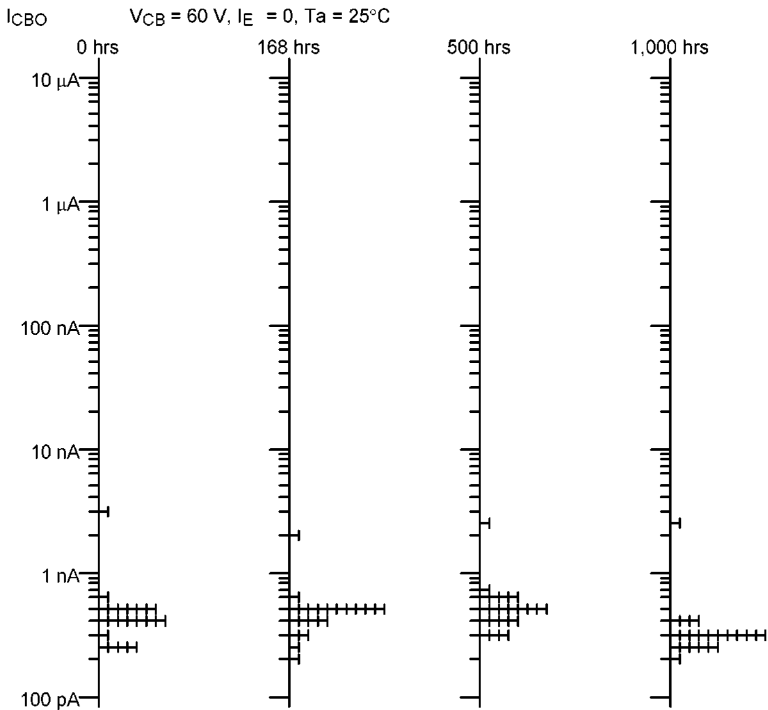


Figure 5.7.17 I_{CBO} results from steady-state operation lifetime test for the 2SD1406 low-frequency power amplification transistor

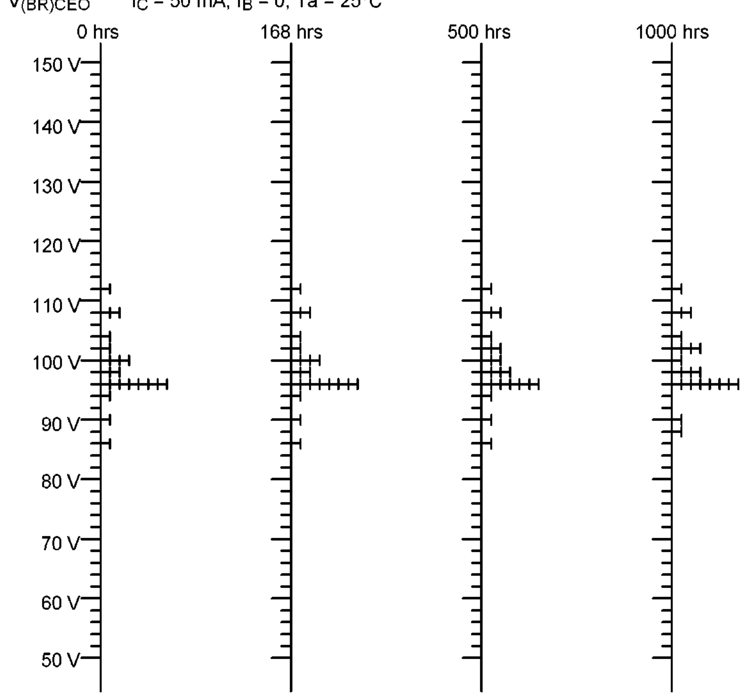


Figure 5.7.18 $V_{(BR)CEO}$ results from steady-state operation lifetime test for the 2SD1406 low-frequency power amplification transistor

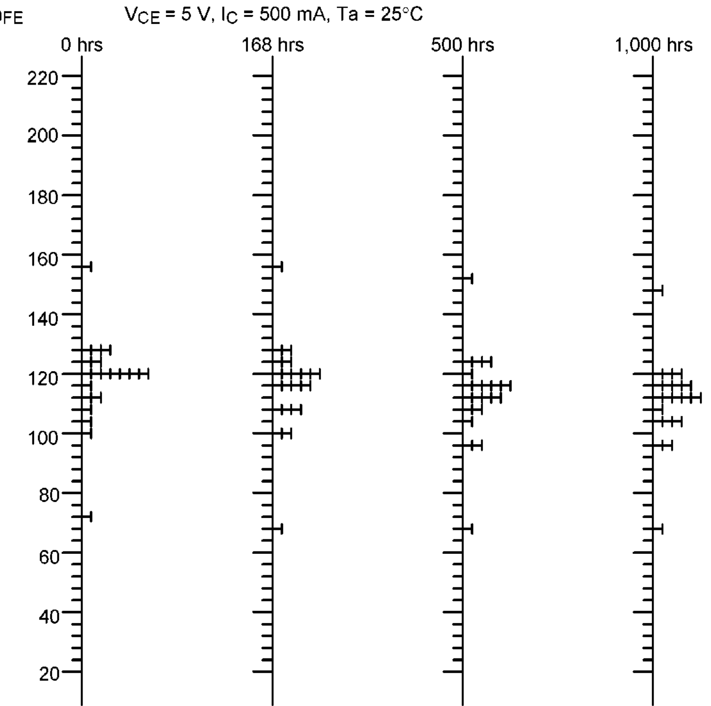


Figure 5.7.19 Transistor h_{FE} results from steady-state operation lifetime test for the 2SD1406 low-frequency power amplification transistor

(2) Reliability characteristics (thermal fatigue test)

- Application circuits which use power transistors usually generate heat due to power loss in the device itself, as described earlier. Consequently, a heat radiation design sufficient to suppress heat to the derated junction temperature must be determined based on the device's absolute maximum ratings. Depending on the application circuit, however, the usage duty (the number of times the device switches on and off within a period of time) may be more important than the conduction time. In such cases, reliability is measured by the yardstick referred to as the thermal fatigue test (TFT).
- The thermal fatigue test (TFT) is generally used to evaluate the effects of change in the case temperature (or junction temperature) combined with repeated on-off cycling. The test is performed in an environment that simulates actual working conditions by turning the power on and off repeatedly within a short period of time (1 ~ 3 minutes) while forced cooling is applied.
- Failure modes in the test include ① degradation of the chip mounting, ② chip cracking, and ③ bonding faults. These failures are thought to be due to the differences between the thermal expansion coefficients of the materials used in the construction of the power transistor (e.g. the silicon of the chip, the molding material, solder and chip coating material) causing internal mechanical stress in the device.

- Figure 5.7.20 shows TFT data for a 2SD1406 transistor housed in a TO-220 (IS) package. At junction temperature ΔT_j = 100°C, 10% defects occur after about 300k cycles (the device is turned on and off 300,000 times).

  The 2SD1406 is designed for general-purpose applications at a rated voltage of 60 V at 3 A. A common application is as a series regulator. Assuming that it is applied in a typical household TV under the following conditions:

  $$\left[\begin{array}{ll} T_j(\max) \leq 120°C, & Ta(\max) = 60°C \\ \text{Set life} = 5 \text{ years}, & \text{Usage frequency} = 5 \text{ times / day} \end{array}\right]$$

  ΔT_j = 60°C and n = 9k cycles is required.

  Considering the performance capabilities shown in Figure 5.7.20, the 2SD1406 can be used under the conditions given above without problems.

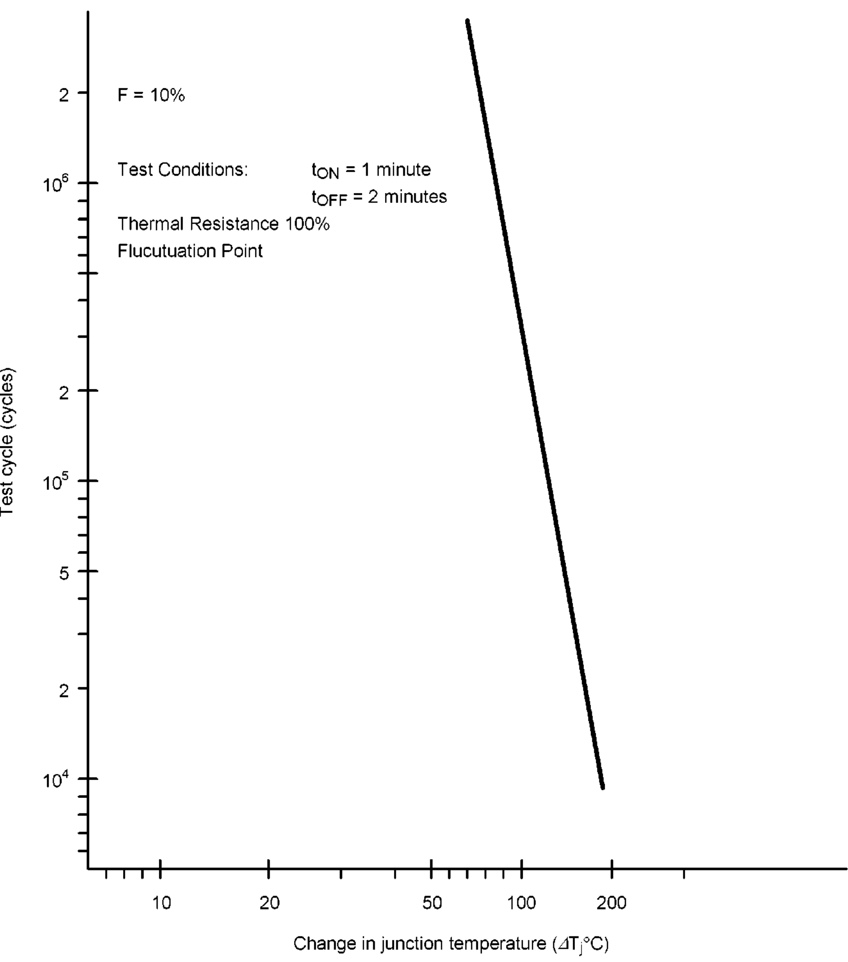


Figure 5.7.20 2SD1406 TFT performance curve

5.8 Power MOSFET Reliability

5.8.1 Overview

(1) Features

In principle, power MOSFETs operate using majority carriers only. Consequently, they are free of the minority carrier problems found in bipolar transistors, such as the storage effect during switching and secondary breakdown. Power MOSFETs are therefore suited to high-speed, low-loss, high-power applications.

① Unlike current-controlled bipolar transistors, MOSFETs are voltage-controlled devices. They are driven by the voltage applied between the gate and the source. Very little power is required to drive MOSFETs.

② As majority carrier devices, MOSFETs do not have a storage time delay (t_{stg}) due to carrier storage effects. They are therefore capable of high-frequency switching.

③ Current concentration in the high-voltage area for bipolar transistors can lead to junction breakdown due to the secondary breakdown phenomenon. Hence, the operating conditions must be carefully taken into account if bipolar transistors are to be used safely. Power MOSFETs do not exhibit the secondary breakdown phenomenon thanks to their on-resistance temperature characteristics. Accordingly, they have a larger safe operating area.

(2) Device types

Power MOSFETs are broadly classified into three types, as shown in Figure 5.8.1.

Figure 5.8.1(a) shows an enhanced version of the small-signal MOSFET which obtains high-voltage tolerance through an ion-implantation process to add a high-resistance layer to its offset gate structure. However, the extended channel length of this structure is reduces the degree of intefration possible.

The MOSFET shown in Figure 5.8.1(b) obtains high voltage tolerance using a V-groove (or U-groove) gate and by forming channels through double-diffusion and anisotropic etching. This structure can cause current concentration at the tip of the groove, making it unsuitable for applications requiring high voltage tolerance. It is used, however, in power MOSFET applications where a low voltage tolerance level is acceptable.

The MOSFET shown in Figure 5.8.1(c), high voltage tolerance can be obtained by the formation of double-diffused channels. This structure is referred to as double-diffusion MOS (DMOS).

With the DMOS structure, the gate area (which becomes the channel) and the source area (doped into high concentration) are diffused on a high-resistance drain substrate through the same diffusion window. This creates a difference in diffusion depth between the two areas, thus forming the channel. The impurity distribution profile derived from the formation of the gate-drain junction shows a smaller concentration on the drain side.

An advantage of the DMOS structure is that when drain voltage is applied, the depletion layer extends further towards the drain side than the channel side. For even a very short channel, this prevents reduced withstand voltage due to punch-through effects, making high voltage-tolerance design possible.

In addition, circuit integration can be increased by devising a structure in which the drain electrode is taken from the reverse side of the substrate; this is advantageous for high-power design. At the same time, since this structure is equivalent to a cascade-connected power MOSFET and junction FET, it helps reduce the feedback capacitance of the power MOSFET.

Unlike the two other types of MOSFET shown in Figure 5.8.1(a) and (b), the DMOS structure allows high voltage tolerance as well as low-cost, high-current designs which can be implemented easily and mass produced. The DMOS structure is widely used in power MOSFETs for standard power amplifier designs.

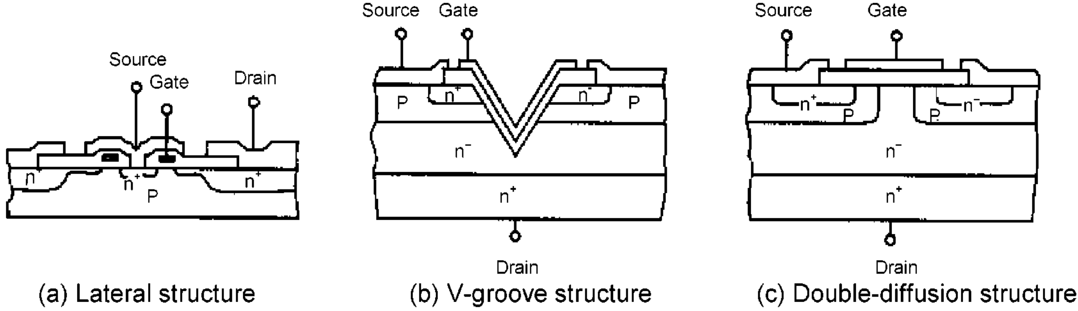


Figure 5.8.1 Power MOSFET structures

(3) Internal structure

Power MOSFETs normally have the source, gate and drain as their internal chip electrodes. Generally, the drain is mounted on a frame that extends directly from the reverse side of the chip to serve as an external lead, while the source and gate are connected to their external leads by bonding wires.

5.8.2 Usage Precautions

(1) Absolute maximum ratings

(a) Drain-to-source voltage absolute maximum rating

There are four ways to stipulate the power MOSFET drain-source breakdown voltage. Which one one selected depends on the gate-to-source bias condition mode. Figure 5.8.2 shows each of these modes.

① V_{DSS}: Voltage between drain and source when the gate-to-source junction is zero-biased (the first “S” in the suffix denotes “short”.)

② V_{DSX}: Voltage between drain and source when the gate-to-source junction is biased (for example, when V_{GS} = −3 V is applied to an N-channel MOSFET.)

③ V_{DSR}: Voltage between drain and source when the gate-to-source junction is shunted with a resistor (the “R” in the suffix denotes “shunt resistor”.)

With a fully enhanced power MOSFET, the relationship $V_{DSS} \approx V_{DSX}$ can be established for each of the three breakdown voltage modes described above. Furthermore, if an arbitrary resistance is inserted between gate and source, the measured drain-to-source breakdown voltage (V_{DSR} mode) should differ little from that of V_{DSX} mode and, hence, it can be established that $V_{DSS} \approx V_{DSX} \approx V_{DSR}$. Consequently, none of the drain-to-source breakdown voltages can be greater than the stipulated V_{DSS} absolute maximum rating. This means that V_{DSS} must never be exceeded, even momentarily.

④ V_{DSO}: Voltage between the drain and source when the gate is open

In V_{DSO} mode, since the input impedance of the power MOSFET itself is very high, the gate-to-source junction may be biased to the ON state by electrostatic induction or other factors, damaging the device. You should therefore not use power MOSFETs in this mode.

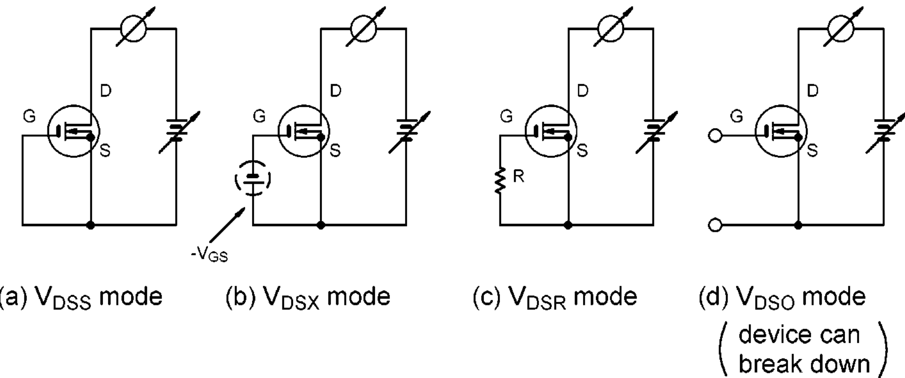


Figure 5.8.2 Drain-to-source breakdown voltages

(b) Gate-source voltage absolute maximum rating

V_{GSS}: Voltage between gate and source when the drain and source are shorted together.

V_{GSS} is attributed to the breakdown voltage of the gate oxide film. The V_{GSS} absolute maximum rating normally stipulated for MOSFETs is ±20 V. This results in a practical voltage amplitude and gives good reliability.

(2) Precautions when using power MOSFETs

(a) Effects of wiring inductance

The switching speed of power MOSFETs is greater than that of bipolar transistors by more than an order of magnitude. They can therefore out-perform most other devices in high-speed switching applications. However, this high-speed switching characteristic can result in a voltage surge when stray inductance Ls is applied to the FET, unless care is taken in the circuit design. The amplitude of Vsurge is

$$Vsurge = -(Ls + L's) \bullet di / dt + V_{DD}$$

This value must have sufficient margin relative to the drain-to-source breakdown voltage V_{DSS}. Furthermore, to repress this value, di/dt or stray inductance must be reduced. Since reducing di/dt is contrary to the original purpose of high-speed switching, the only available method is to reduce the stray inductance.

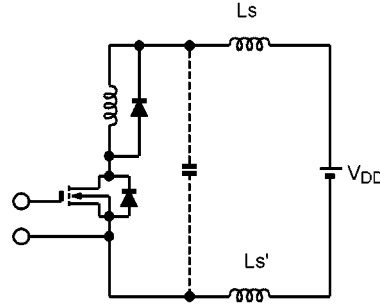


Figure 5.8.3 Stray inductance in circuit

Using copper plating instead of wire reduces inductance significantly. Similarly, the voltage surge can be effectively reduced by inserting a capacitor in the circuit as shown in Figure 5.8.3.

(b) Parasitic oscillation

Power MOSFETs tend toward parasitic oscillation more easily than bipolar transistors. This is attributable to their inherently large high-frequency gain characteristic. Parasitic oscillation occurs when the input-to-output coupling is strengthened by gate-to-drain capacitance (Crss) or stray wiring capacitance (Cs), thereby converting the impedance on the input side to a load resistance. This problem can be prevented as shown in Figure 5.8.4.

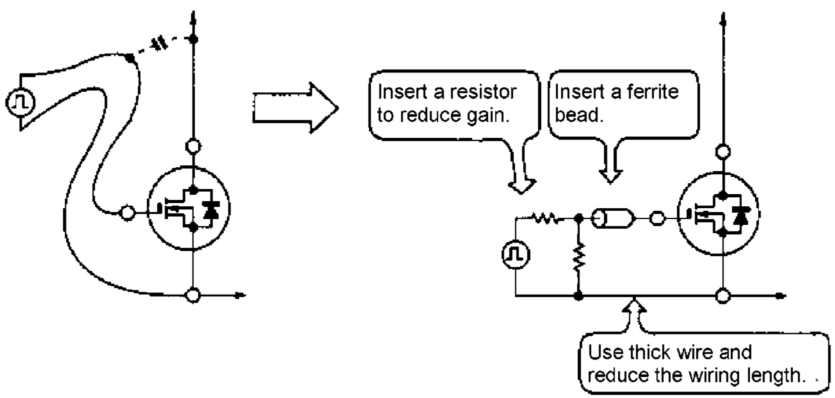


Figure 5.8.4 Methods for preventing parasitic oscillation

① Use thick wire and reduce the wiring length. Use of twisted-pair wiring prevents cross-talk between the gate and drain signals, and other signals.

② Insert a ferrite bead as close to the gate as possible.

③ Insert a resistor in series with the gate.

(c) Applying forward bias to achieve a safe operating area

Unlike bipolar transistors, power MOSFETs do not cause secondary breakdown in high-voltage regions because their structure frees them from the problem of current concentration. The safe operating area (SOA) of a power MOSFET can be expressed in terms of thermal resistance using the equal power load lines shown in Figure 5.8.5, with pulse width as the parameter.

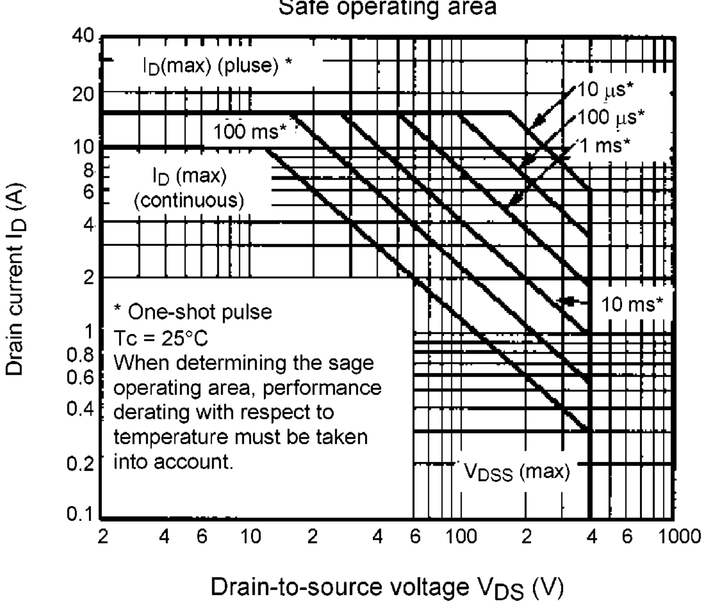


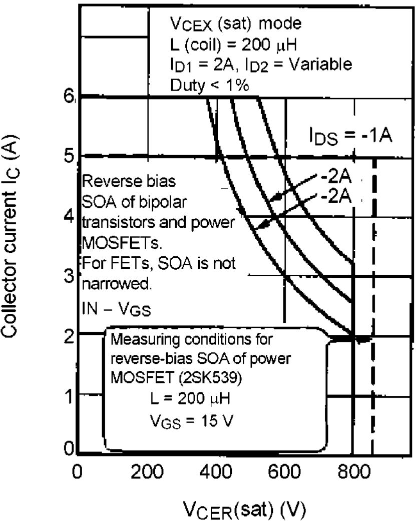
Figure 5.8.5 Safe operating area (SOA) of power MOSFET

Since power MOSFETs do not exhibit a narrowing of the SOA in high-voltage regions, they can be operated safely within the drain-to-source breakdown voltage.

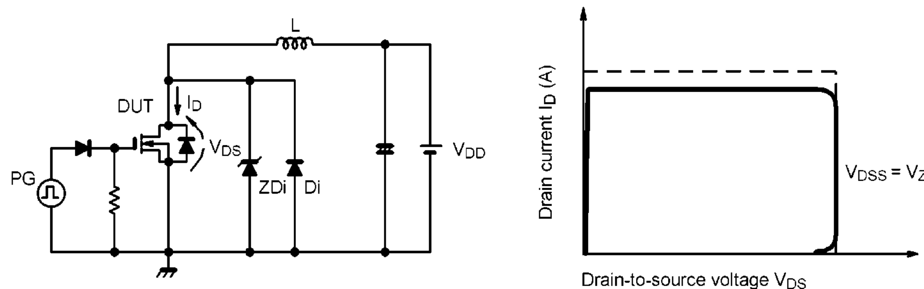
(d) Reverse-bias safe operating area

When switching devices are used in power-switching applications, such as a switching power supply, the load becomes inductive. This presents a problem for a reverse-bias SOA, just as it does for a forward-bias sort.

When bipolar transistors are used in switching power supplies, switching loss is usually reduced by forcibly reverse-biasing the base-to-emitter junction in order to reverse the flow of base current I_{B2} and thus reduce t_{stg} and t_f. However, if I_{B2} increases, the reverse-bias SOA narrows, as shown in ｴﾗｰ! 参照元が見つかりません。, thus limiting the load line operating range at the time that the device is switched off.



(a) Reverse-bias SOA of bipolar transistors



(b) Reverse-bias SOA measuring circuit and load locus waveform

Figure 5.8.6 Reverse bias safe operating area

For power MOSFETs too, you can reduce t_f and t_{off} by reverse-biasing the gate-to-source junction. Since power MOSFETs are majority-carrier devices and inherently free from carrier storage effects, they do not suffer from a narrowing of the reverse-bias SOA when the gate reverse voltage V_G increases.

(e) Source-to-drain diode

A power MOSFETs with the double-diffused structure contains an equivalent diode between source and drain. The tolerance ratings for the diode forward current I_{DR} (Figure 5.8.6) and reverse breakdown voltage are the same, respectively, as those for the drain current I_D and drain-to-source voltage V_{DSS} of the power MOSFET.

The reverse recovery time t_{rr} of the equivalent diode is comparable to that of a fast recovery diode (FRD). Figure 5.8.7 shows a typical circuit used to measure the reverse recovery time of the equivalent diode in a power MOSFET.

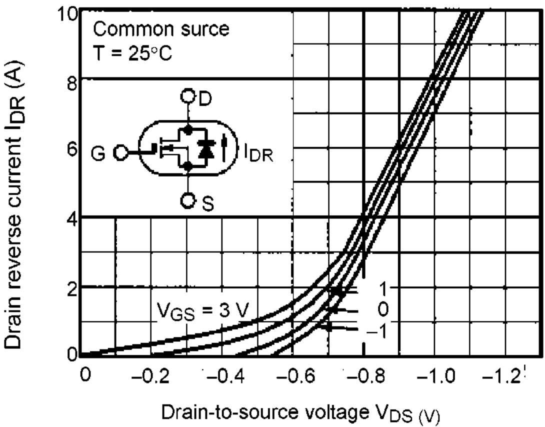


Figure 5.8.6 I_{DR} vs. V_{DS} characteristics

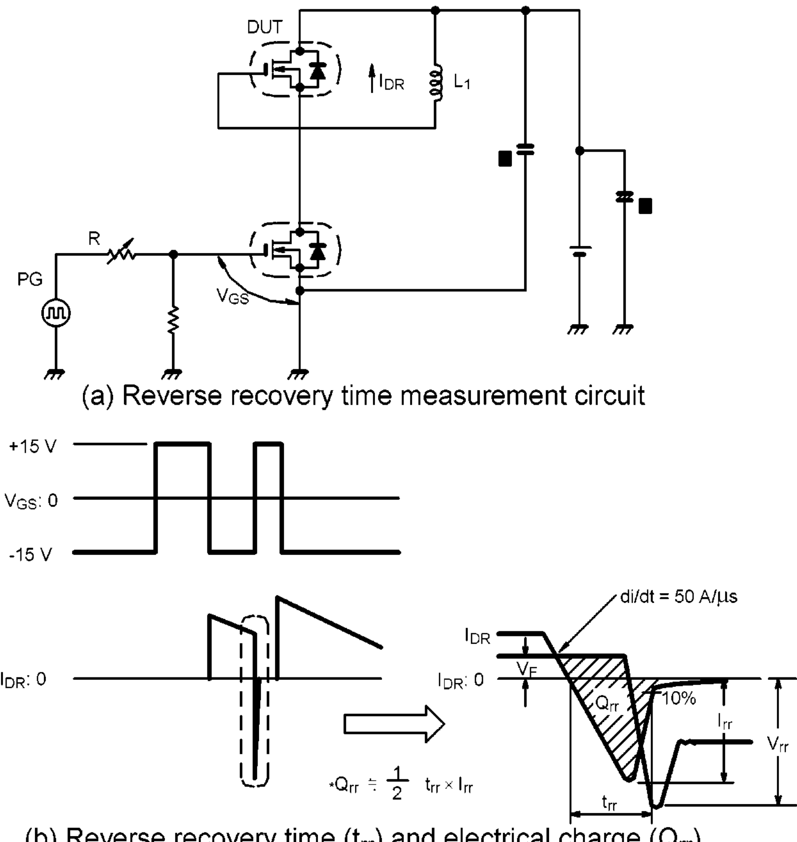


Figure 5.8.7 Circuit for measuring the reverse recovery time of the equivalent diode in a power MOSFET

Power MOSFETs in motor control circuits are generally used in a bridge configuration with upper and lower devices that turn on and off alternately.

Assume in Figure 5.8.8 that power MOSFETs Q_1 and Q_4 turn on, allowing current A to flow. When FETQ_1 turns off to control the motor speed, current B flows back through the flywheel diode in FETQ_2. When FETQ_1 turns on again, a short-circuit current flows from FETQ_1 to FETQ_2 for a duration of t_{rr} until the flywheel diode of FETQ_2 reverse-recovers, generating heat due to power loss. Consequently, when using power MOSFETs for motor control, you should choose devices whose equivalent diodes have a short t_{rr}. Although in principle the internal equivalent diode of a power MOSFET can be used as the flywheel diode, depending on the operating conditions some applications may require an external diode as shown in Figure 5.8.9.

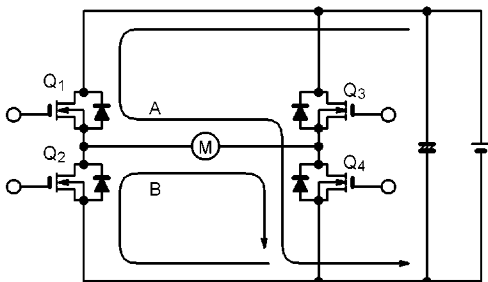


Figure 5.8.8 Motor control circuit using power MOSFETs

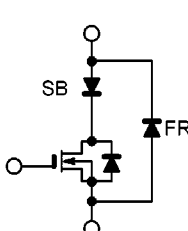


Figure 5.8.9 Method for connecting an external diode

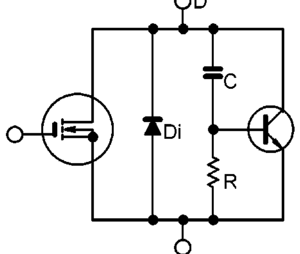
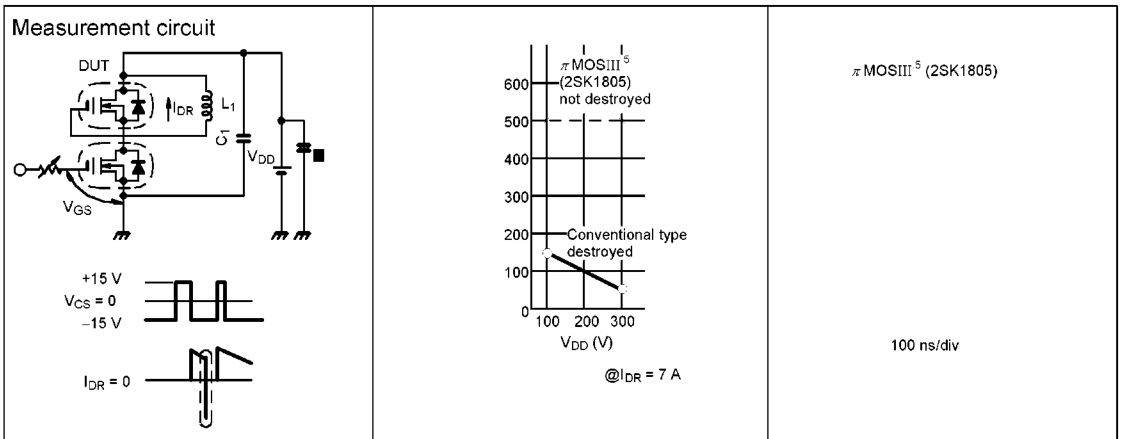


Figure 5.8.10 Parasitic transistors in power MOSFETs

In addition to the above problems, power MOSFETs also contain an equivalent parasitic bipolar transistor between the drain and the source, as shown in Figure 5.8.11. In the MOSFET transition state (from ON to OFF), the voltage drop due to the resistance R between base and emitter causes the parasitic transistor to turn on, leading to a breakdown of the device. The presence of this parasitic transistor must therefore be taken properly into account.

When using the internal equivalent drain-to-source diode of a power MOSFET in a motor control application, power supply application or inverter lighting application, it is recommended that you use a rugged device type such as a menber of the ϕ-MOS III^5 Series. This will ensure superior destruction-proof performance, as shown below.

Destruction-proof performance of the internal diode (high-capacity internal diode device)



Typical internal high-strength diode device types: 2SK1574, 2SK1805, 2SK1864, 2SK1488, 2SK1855, 2SK1865, 2SK1745, 2SK1856 etc.

(f) About parallel connections

Since power MOSFETs are free fom thermal runaway and exhibit excellent thermal stability, parallel connections are easier than with bipolar transistors.

Because bipolar transistors are driven using the base current, they are susceptible to collapsed current balance due to variations in base-to-emitter voltage V_{BE}. Parallel connections with bipolar transistors are therefore problematic. Conversely, because power MOSFETs are voltage driven, their operation requires only that a drive voltage be appied to each parallel-connected FET, making parallel connections much easier with power MOSFETs. However, when controlling high power at high speed, it is important to choose the appropriate device and to consider variations in device characteristics. It is particularly important to avoid current concentration, even during transient states, when connecting devices in parallel, so as to ensure that current flows evenly to all devices under all load conditions.

Generally, unbalanced current usually occurs at ON and OFF switching transitions. This is attributable to variations in the switching time of power MOSFETs. This variation is known to depend largely on the gate-to-source threshold voltage V_{th}. That is, the smaller the V_{th}, the faster the MOSFET turns on; and the larger the V_{th}, the slower the MOSFET turns on. It has also been observed that the larger the V_{th}, the faster the MOSFET cut-off speed; and the smaller the V_{th}, the slower the cut-off speed. From this observation, it can be assumed that current imbalance occurs because current concentrates in FETs whose V_{th} is small at both turn-on and turn-off. This king of a current imbalance can cause excessive power dissipation in the device, leading to breakdown. Thus, taking into account the variations in switching times at transitions, the V_{th} of all parallel-connected power MOSFETs should be equal.

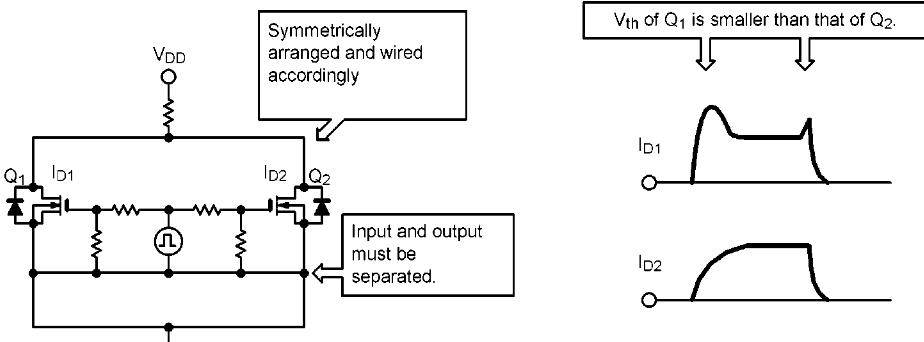


Figure 5.8.11 Current imbalance in parallel-connected MOSFETs

5.8.3 Reliability Characteristics

(1) Reliability test results

As an example of reliability-testing, Table 5.8.1 shows results of reliability tests performed using a plastic-encapsulated power MOSFET.

Table 5.8.2 lists examples of failure criteria applied during the test.

A basic method for evaluating reliability is to have a device in operation and to perform a detailed analysis of how its characteristics change over time. As an example, Figure 5.8.12 to 5.8.17 show the changes in characteristics for a device subjected to the lifetime test described in Table 5.8.1.

Test results indicate that, although the device was operated as its absolute maximum ratings, the initial characteristics remained stable over a long period of time.

Consequently, this device can be expected to offer high reliability in an application.

Table 5.8.1 Reliability test results for the 2SK1124 power MOSFET

	Test	Applicable Standard JIS C7021	Test Conditions	No. of Devices Test	No. of Devices Failures
Lifetime tests	Steady-state operation	B-4	P_D = 8.8 W (heat sink used) Ta = 25°C, 1,000 hrs	30	0
	High-temperature reverse bias	B-8	Ta = 150°C, V_{GS} = 20 V 1,000 hrs	30	0
	High-temperature storage	B-10	Ta=150°C, 1,000 hrs	30	0
	High-temperature high-humidity storage	B-11	Ta = 60°C, RH = 90% 1,000 hrs	30	0
Environment tests	Soldering heat	A-1	260°C, 10 secs, once (immersed 1.5 mm from device base)	32	0
	Temperature cycling	A-4	–55°C to 25°C to 150°C to 25°C 100 cycles	50	0
	Thermal shock	A-3	100°C to 0°C, 50 cycles	32	0
	Moisture resistance	A-5	Ta = to 65°C, RH = 90% to 98% 10 cycles	32	0
Mechanical tests	Vibration	A-10	100 to 2,000 Hz 196 m/s^2 4 times each in 3 directions	11	0
	Mechanical shock	A-7	0.5 ms, 14,700 m/s^2 (1500 G) 3 times each in 4 directions	11	0
	Constant acceleration	A-9	196,000 m/s^2 1 minute each in 6 directions	11	0
	Lead integrity	A-11	500 g, bent 90° 3 times	11	0
	Dropping	A-8	75 cm, on maple board, 3 times	11	0
	Solderability	A-2	230°C, 5 secs (using designated flux)	11	0

Table 5.8.2 Failure Criteria for 2SK1124

Parameter	Symbol	Measuring Conditions (Ta=25°C)	Criteria	
			minimum	maximum
Gate leakage current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	USL × 2
Drain cut-off current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0	—	USL × 2
Drain-to-source breakdown voltage	V_{DSS}	I_D = 10 mA, V_{GS} = 0	LSL × 0.9	—
Drain-to-source on-resistance	R_{DS}(ON)	I_D = 25 A, V_{GS} = 10 V	—	USL × 1.2

USL: Upper specification limit; LSL: Lower specification limit

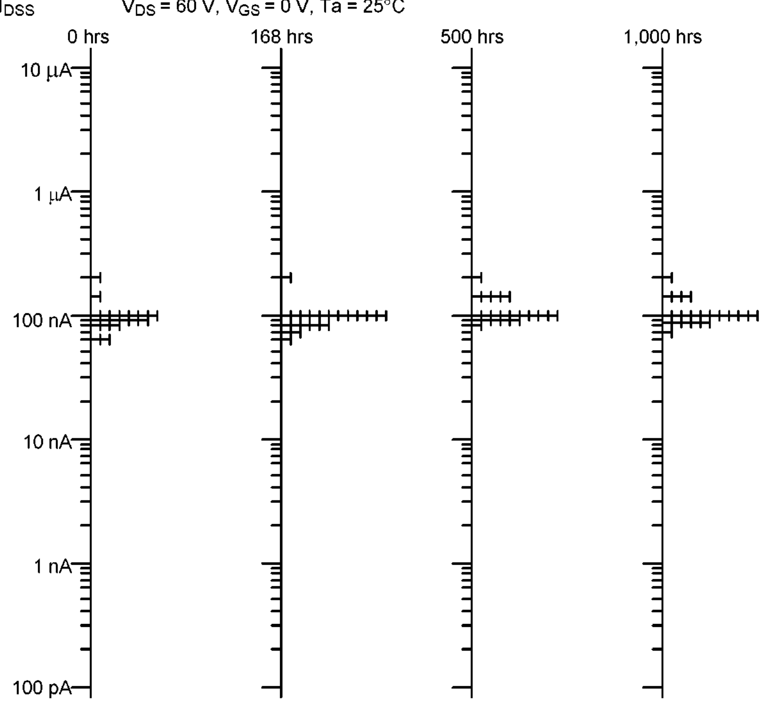


Figure 5.8.12 I_{DSS} results from steady-state operation lifetime test for the 2SK1124 power MOSFET

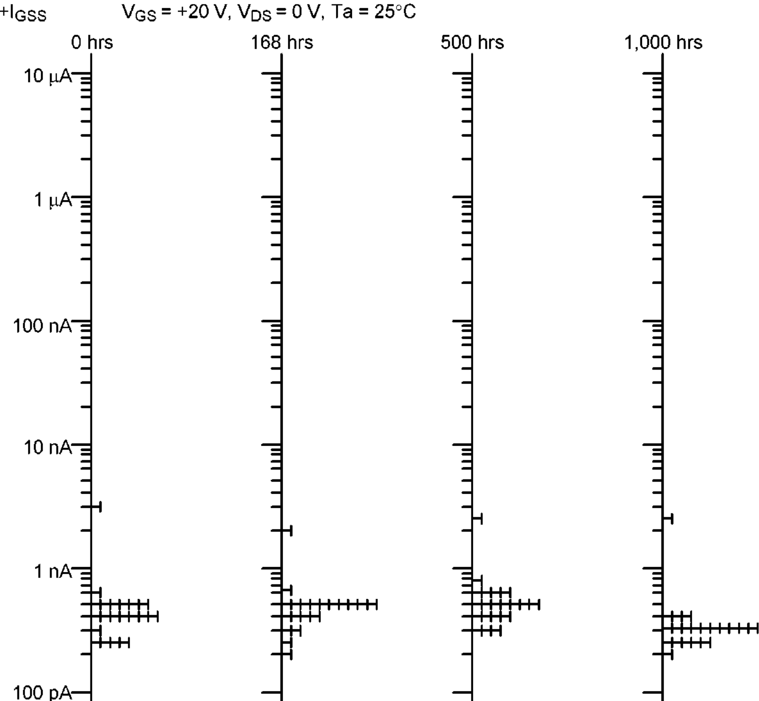


Figure 5.8.13 +I_{GSS} results from steady-state operation lifetime test for the 2SK1124 power MOSFET

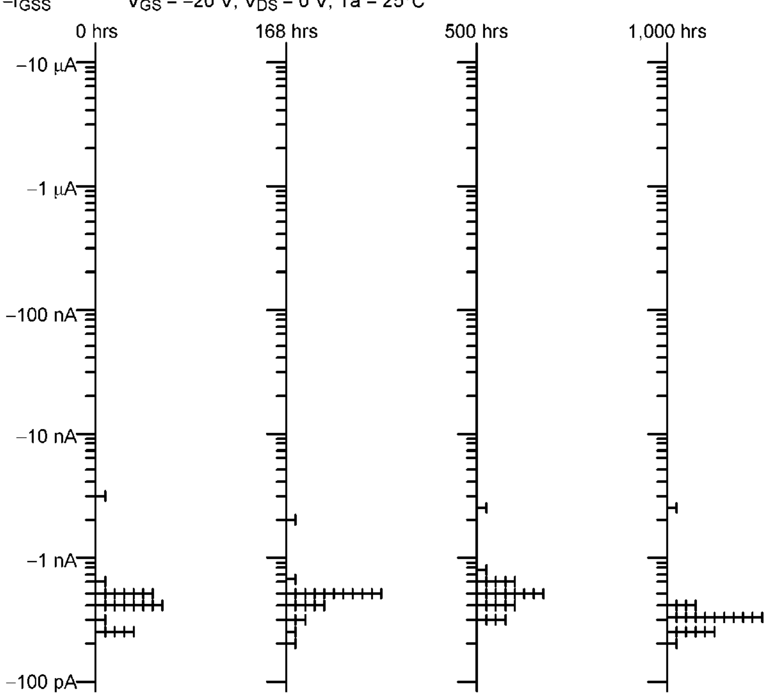


Figure 5.8.14 -I_{GSS} results from steady-state operation lifetime test for the 2SK1124 power MOSFET

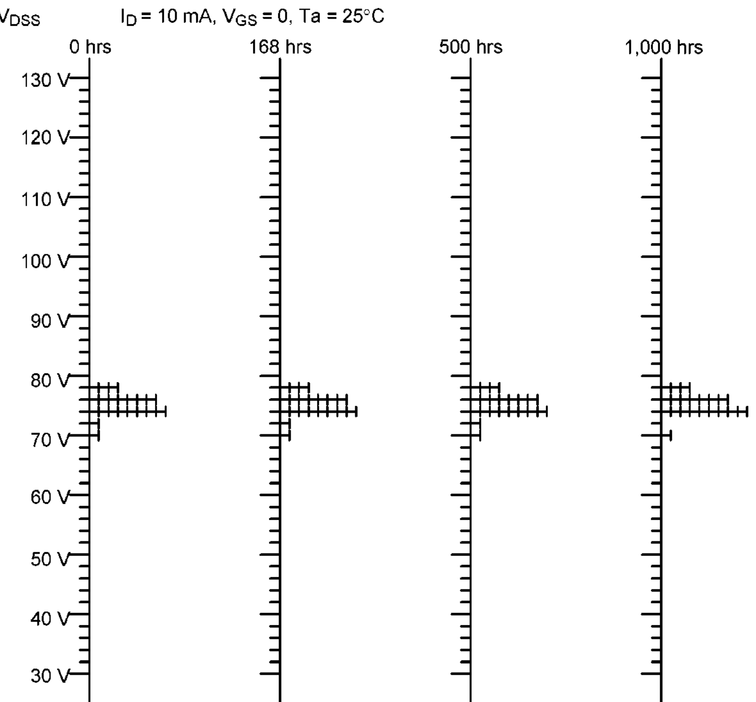


Figure 5.8.15 V_{DSS} results from steady-state operation lifetime test for the 2SK1124 power MOSFET

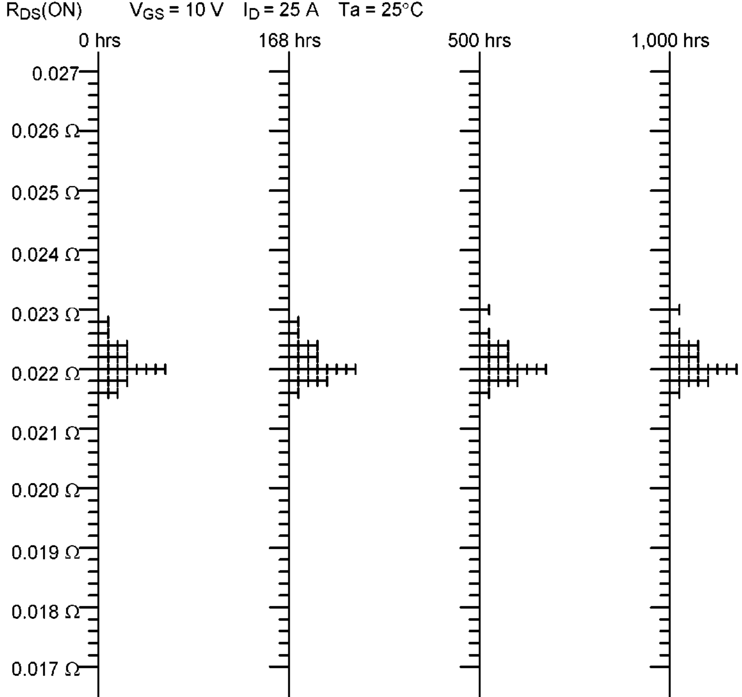


Figure 5.8.16 R_{DS} results from steady-state operation lifetime test for the 2SK1124 power MOSFET

(2) Reliability characteristics (oxide film breakdown over time)

The gate electrodes of power MOSFETs are insulated with thin oxide film. Although the intrinsic breakdown voltage of the oxide film can reach as much as 10 MV/cm, that of ordinary oxide film is usually closer to 6 MV/cm ~ 8 MV/cm. This means that for a gate oxide film thickness of about 1000 Å, the breakdown voltage is around 60 V ~ 80 V.

However, even when the applied voltage is below the dielectric breakdown level, over time the oxide film insulation degrades, leading to an eventual breakdown when it is subjected to a strong electrical field. This phenomenon is referred to as time-dependent dielectric breakdown (TDDB).

Figure 5.8.17 is an example showing the lifetime of an actual power MOSFET relative to the TDDB phenomenon. The diagram shows how, at low temperature, when the applied voltage between the gate and the source is reduced, the lifetime of the power MOSFET is extended proportionately. In this example the lifetime of the power MOSFET can be is lengthened by as much as 20 times by lowering V_{GS} by around 5 V. This suggests that for applications where reliability is critical, care must be taken not to set the gate-to-source voltage unnecessarily high.

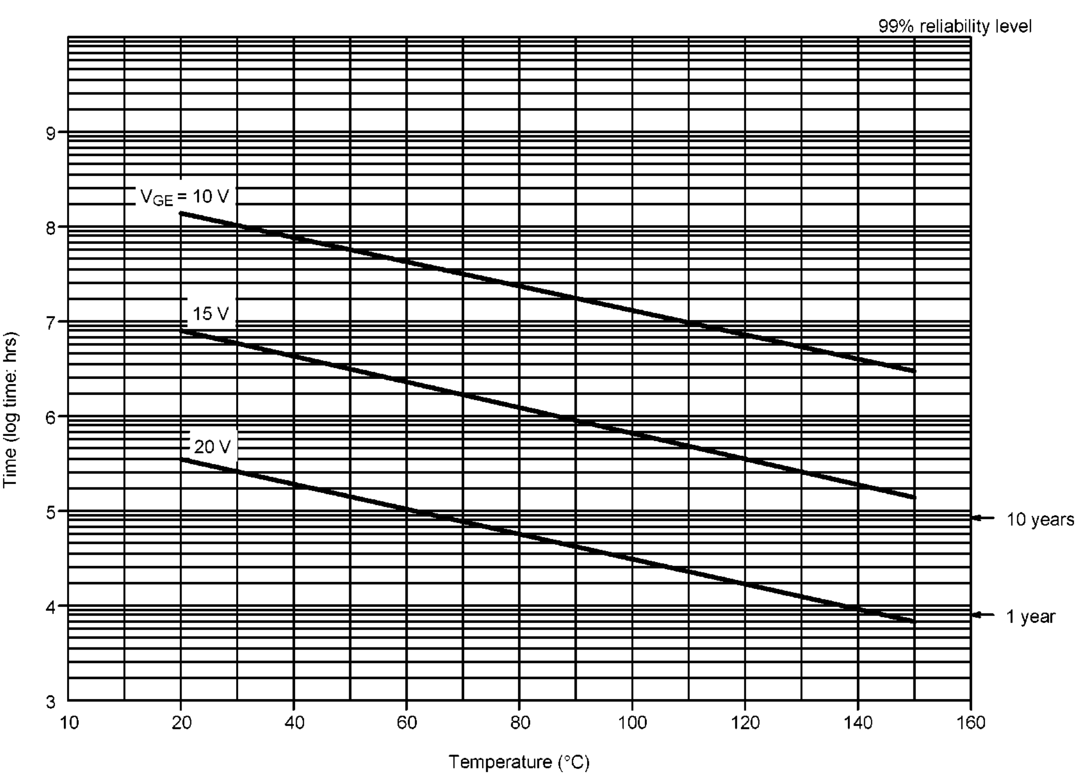


Figure 5.8.17 Life of gate oxide film for the 2SK1124 power MOSFET

5.9 IGBT Reliability

5.9.1 Overview

(1) Features

Insulated-gate bipolar transistors (IGBTs) combine the high input impedance and high-speed characteristics of MOSFETs and the high-conduction (low saturation voltage) characteristics of bipolar transistors. The structure of an IGBT is very much like that of the Toshiba π-type MOSFET shown in Figure 5.9.1. The difference is the N^+-N^- substrate used in MOSFETs, as opposed to the P^+-N^- type used in IGBTs. The IGBT fabrication steps following the substrate process are therefore basically the same as those for MOSFETs. Figure 5.9.2 shows an equivalent circuit for the IGBT structure and its device symbols.

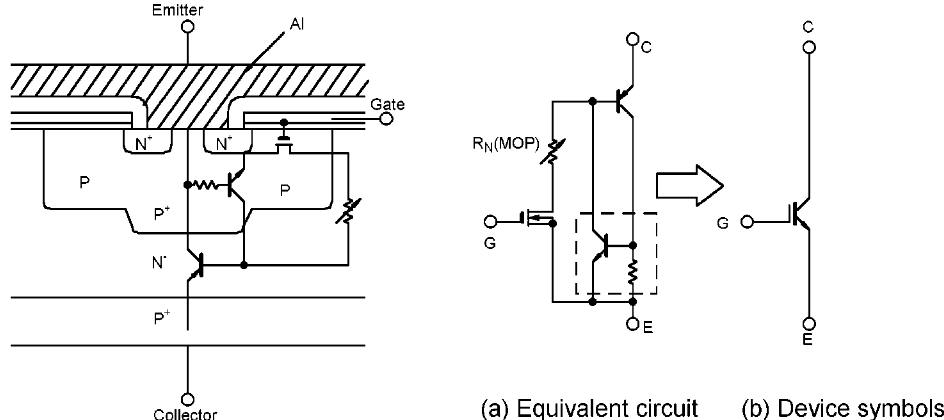


Figure 5.9.1 Basic structure of an IGBT

Figure 5.9.2 Equivalent circuit and device symbols for IGBT

The thyristor formed by the PNP-NPN transistor coupling in the equivalent circuit shown in Figure 5.9.2 has its base and emitter shorted by aluminum patterning to prevent it from operating, and is therefore considered irrelevant to the basic operation of the IGBT. Consequently, the equivalent circuit and basic operating mechanism of an IGBT are the same as those of a MOS-input inverted darlington transistor comprised of an N-channel enhancement MOSFET in the input stage and a PNP transistor in the output stage.

To turn on an IGBT, first gate voltage is applied to form a channel, then the base current of the PNP transistor is supplied to inject the minority carrier into the N^- layer region. Conversely, to turn off an IGBT, the channel is removed to shut down the base current until all minority carriers are gone. Thus, IGBTs are driven in exactly the same way, and have the same high input impedance characteristics, as MOSFETs.

(2) Packages

IGBTs come in various packages - SMD, TO-3P (L), SIP and MODULE - as appropriate to their intended application. These packages are illustrated in Figure 5.9.3 to 5.9.6.

(a) SMDs are used for configuring inverter circuits requiring relatively small current capacity, such as in a hybrid IC. (See Figure 5.9.3.)

(b) A TO-3P (L), a printed circuit board insertion type device, is used in household equipment applications requiring relatively small current capacity (8 A to 60 A). (See Figure 5.9.4.)

(c) A SIP is a package for a three-phase inverter circuit configured using six IGBTs. It can be installed easily on printed circuit boards, although the current capacity is slightly less than that the TO-3P (L) type described above. (See Figure 5.9.5)

(d) A MODULE consists of IGBTs mounted on a Direct Bond Copper (DBC) board for insulation purposes and can be fitted to a heat sink easily. Standardized for a rated current of up to 600 A, this package type is particularly suited to high-power applications. (See Figure 5.9.6.)

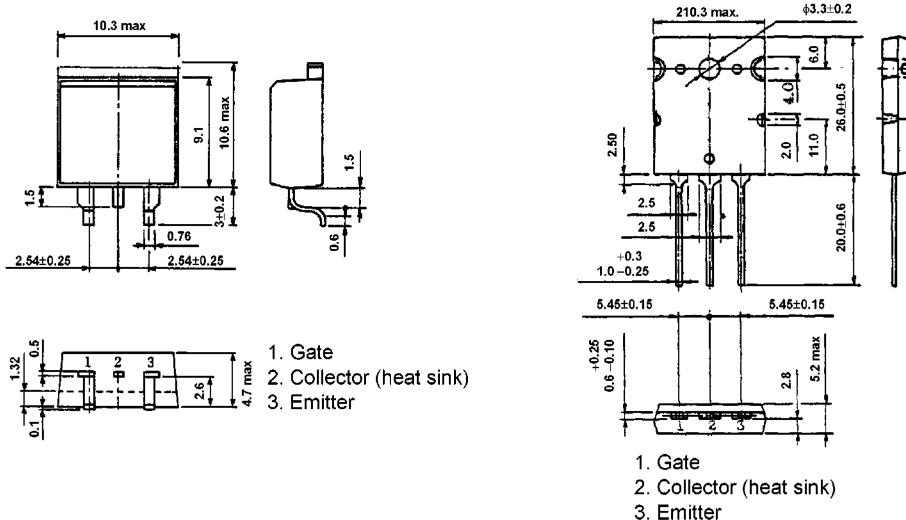


Figure 5.9.3 Example of an SMD package

Figure 5.9.4 Example of a TO-3P (L) package

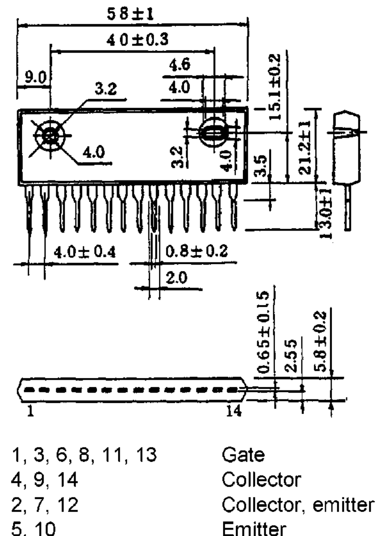


Figure 5.9.5 Example of a SIP package

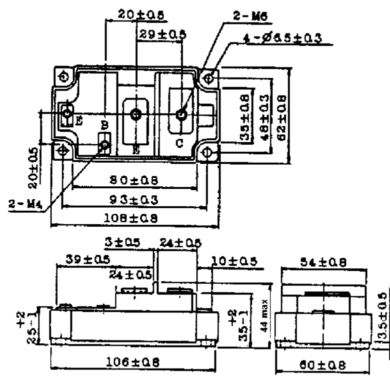


Figure 5.9.6 Example of a MODULE package

5.9.2 Usage Precautions

(1) Absolute maximum ratings

(1.1) Definition of absolute maximum ratings

Maximum permissible values for current, voltage and power dissipation in IGBTs are stipulated as absolute maximum ratings.

When designing application circuits using IGBTs, a good understanding of IGBT absolute maximum ratings is important to ensure that the devices operate efficiently and reliably.

Semiconductor devices such as IGBTs are characterized by the fact that their electrical characteristics are very sensitive to temperature. Absolute maximum ratings are specified in order to guard against problems which could arise as a result of device temperature sensitivity. For example, a rise in the ambient temperature while a certain voltage is applied to an IGBT will increase the leakage current, resulting in increased power consumption in the IGBT. This will cause a further rise in temperature, which will cause a further increase in the leakage current, and so on, leading to a vicious cycle that can eventually cause the IGBT to break down.

To guarantee a useful lifetime and the reliability of an IGBT, no absolute maximum rating must ever be exceeded, even momentarily. These values are stipulated according to the material, design and manufacturing conditions of the IGBT type and package.

Furthermore, absolute maximum rating values for any two or more parameters must not be applied to the IGBT simultaneously.

If an IGBT is used under conditions that exceed the absolute maximum ratings, its characteristics can be degraded to an unrecoverable level. Therefore, when designing circuits, you should consider all factors that can cause absolute maximum ratings to be exceeded, such as fluctuations in the supply voltage, variations in the characteristics of electrical components, circuit adjustments, changes in ambient temperature and fluctuations in input signals.

The primary IGBT absolute maximum ratings include the current in each lead (emitter, gate and collector), voltages across the leads, power dissipation, junction temperature and storage temperature. These characteristics are closely interrelated (in such a way that they cannot be considered in isolation) and vary according to external circuit conditions.

(1.2) Voltage ratings

IGBT input/output circuits are configured so that the emitter electrode is a common terminal. Stipulated voltage ratings, two of which are described below, include the collector-to-emitter and gate-to-emitter voltages as well as the bias relationships between terminals.

V_{CES} : This is the maximum collector-to-emitter voltage when the gate is shorted. Unlike in bipolar transistors, it does not vary with the gate bias, so the relationship $V_{CES} \approx V_{CER} \approx V_{CEX}$ can usually be established.

V_{GES} : This is the maximum gate-to-emitter voltage when the collector is shorted. It is related to the withstand voltage capability of the gate oxide film. The VGES maximum rating is normally stipulated as ±20 V. This results in a practical voltage amplitude and gives good reliability.

(1.3) Current ratings

Maximum current ratings are normally stipulated for $I_F$max (flywheel diode current) and $I_C$max, which flow in the collector electrode. They are determined for an IGBT taking the following into account:

① The current at the specified saturation voltage
② The current at the specified forward voltage (for flywheel diodes, the forward voltage.)
③ The current at which the internal lead wire melts

(1.4) Temperature ratings

The maximum junction temperature Tj(max) depends on the materials from which the IGBT is fabricated. This rating must be considered not only in terms of device operability, but also in relation to reliability factors such as degradation and expected lifetime.

Degradation in IGBTs generally accelerates as the junction temperature increases. It is known that average lifetime Lm (hours) and junction temperature T_j (K) have the following relationship, where A and B are special IGBT constants.

$$\log(Lm) = A + \frac{B}{T_j} \quad \cdots\cdots (1)$$

The guaranteed lifetime of a device therefore depends on the junction temperature upper limit determined in accordance with failure rate and reliability. This is set at 150°C for IGBTs.

Storage temperature T_{stg} stipulates the temperature range within which devices can be safely stored while not in operation. It is determined by the characteristics and reliability of the constituent materials and is set at 125°C for IGBTs.

(1.5) Power rating

Power is dissipated from an IGBT by being converted to thermal energy. This causes the internal temperature of the device to rise.

The internal power dissipation of an IGBT at a certain operating point is determined as follows:

collector dissipation $P_C = I_C \cdot V_{CE}$.

The maximum power dissipation P_C(max) of an IGBTs is limited by several parameters. These are the maximum junction temperature Tj(max), described above, and the reference temperature To the ambient temperature Ta or case temperature Tc). It is known that these parameters are related to thermal resistance R_{th} as follows:

$$P_C\text{max} = \frac{T_{j\text{max}} + To}{Rth} \quad \cdots\cdots \quad (2)$$

Thermal resistance is a physical quantity indicating the propensity of the junction temperature to rise per unit amount of power dissipation; in other words, it describes the ability of a device to radiate heat. For large power dissipation, the IGBT must have a large $P_C$max. Good heat radiation design is extremely important, especially for IGBTs that handle large currents.

(2) Precautions for circuit design

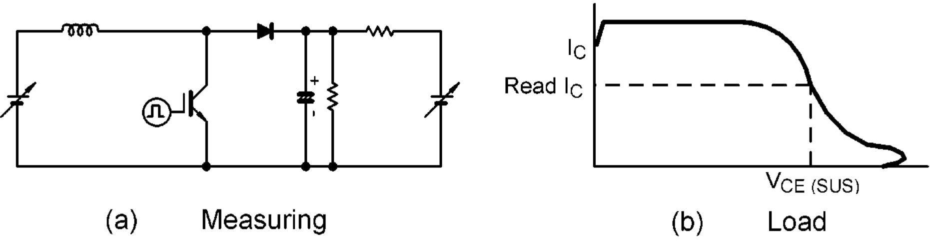
(2.1) Collector-to-emitter voltage V_{CES}

The collector-to-emitter voltage is measured after shorting the gate and emitter to one another.

If it exceeds the break-over voltage, fault symptoms, such as degraded voltage tolerance, can appear. The applied voltage must therefore not exceed the maximum rating.

(2.2) Collector-to-emitter sustaining voltage V_{CEX}(SUS)

The collector-to-emitter sustaining voltage is measured using the circuit shown in Figure 5.9.7.



(a) Measuring (b) Load

Figure 5.9.7 Measuring $V_{CE\ (SUS)}$

V_{CE}(SUS) varies with measurement, read-out and base bias conditions. For a small collector current especially, V_{CE}(SUS) will be small since the reactance energy is insufficient to generate the junction capacitance in the P-N junction of the IGBT.

(2.3) Safe operating area

The operating range within which IGBTs can be used safely without fear of breakdown or degradation is referred to as the safe operating area (SOA).

The operating range of IGBTs is normally limited by their absolute maximum ratings, including maximum voltage, maximum current and maximum collector dissipation. IGBTs used in circuits with inductive loads, however, can degrade or break down even if operated within their absolute maximum ratings. This is attributable to a phenomenon in IGBTs known as secondary breakdown (S/B).

① Secondary breakdown (S/B) phenomenon

The secondary breakdown (S/B) phenomenon occurs when certain voltage-current points ($V_{S/B}$, $I_{S/B}$) are reached (as the current continues to increase after a primary breakdown) and the collector-to-emitter voltage drops rapidly. This causes a transition into the low-impedance region (within 3 or 4 μs) as shown in Figure 5.9.8, often resulting in breakdown of the IGBT.

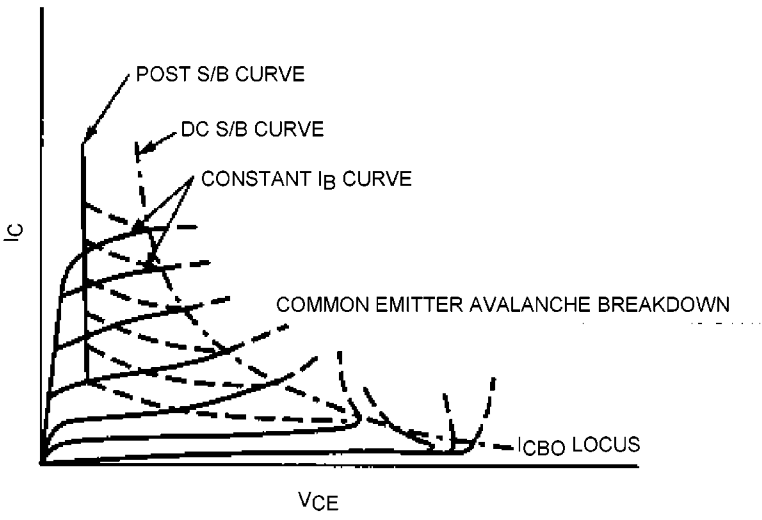


Figure 5.9.8 Collector output characteristics and S/B curves

② Forward-bias SOA (FBSOA)

When the gate-to-emitter junction is positively biased and the collector-to-emitter voltage is low, the collector current flows mostly in the channel area immediately below the gate and secondary breakdown does not occur. When the collector-to-emitter voltage rises, however, the collector current in the parasitic transistor can increase, resulting in secondary breakdown.

③ Reverse bias SOA (RBSOA)

When the gate-to-emitter is negatively biased, current flow in the channel area immediately below the gate ceases, allowing load current to pass through the parasitic transistor.
Since the base of the parasitic transistor is always positively biased, reverse-bias SOA in IGBTs is not dependent on gate bias as is the case with bipolar transistors.

The reverse-bias SOA is measured using the circuit shown in Figure 5.9.9.

Peak voltage V_{CE} is suppressed with a clamping circuit which changes the pulse width of the DC power supply or gate signal in order to set the collector current I_C.

The reverse-bias SOA can be obtained by plotting the measured points.

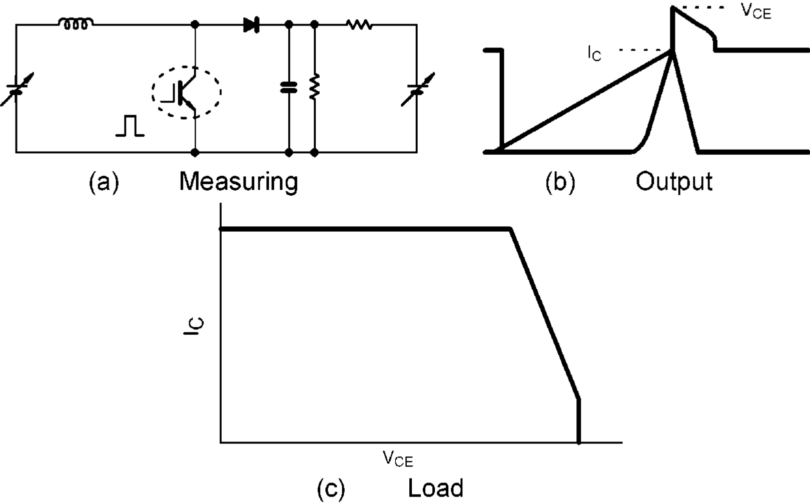


Figure 5.9.9 Reverse-bias SOA

(2.4) Latch-up

When a current that exceeds the rated current flows in an IGBT for a short time only, the device will not normally break down.

However, if the applied gate-to-emitter voltage is sufficiently high, such that the sum of parasitic transistor injection efficiencies ($\alpha_{PNP} + \alpha_{NPN}$) for the induced current is greater than 1, the IGBT will act as a thyristor and will be unable to turn off, even when the gate-to-emitter voltage goes negative. This phenomenon is called latch-up. If there is a large power dissipation when latch-up occurs, the IGBT may break down. If the power dissipation is small, the IGBT can be operated without fear of breakdown, provided that voltage is applied only after the junction temperature has been lowered by reducing the collector current to zero by some other means.

(2.5) Switching characteristics

IGBTs are used mainly as switches in chopper and inverter circuits.

When an IGBT is used in this type of application, the load always includes reactors or other inductive components and the IGBT's turn-on / turn-off switching characteristics can deviate rather widely from the electrical characteristics listed in the IGBT's datasheet.

Figure 5.9.10 shows the turn-on and turn-off waveforms for an IGBT in an inverter circuit.

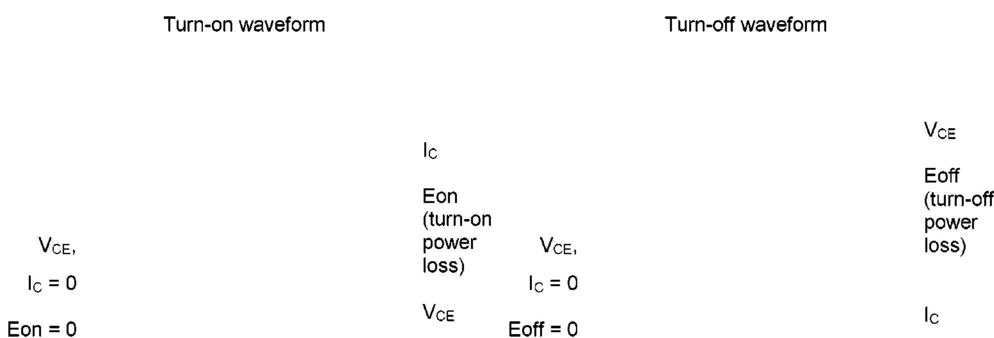


Figure 5.9.10 Switching waveforms for the MG50J2YS1

When a turn-on signal is applied to the IGBT, the collector current first increases and then peaks, then the collector-to-emitter voltage drops.

When a turn-off signal is applied to the IGBT, the collector-to-emitter voltage increases until it exceeds the supply voltage, then the current decreases.

The collector-emitter voltage during the current increase and the overshoot at turn-off time are not determined by the IGBT alone but also by the circuit's wiring inductance. It is therefore important to minimize wiring inductance in the circuit. It is also necessary to evaluate the IGBT under actual mounted conditions when calculating its switching losses (E_{ON} and E_{OFF}).

(2.6) Rate of rise of collector current (di/dt)

The di/dt of an IGBT is determined by its gate drive conditions and is not limited by the turn-on characteristic of the IGBT. However, if di/dt becomes large, the diF/dt of the fast-recovery diode (FRD) increases simultaneously such that an overvoltage can be generated by the FRD, or the FRD can break down due to back power.

For an IGBT to be used safely, di/dt must be lowered. However, excessive lowering increases the turn-on power loss (Eon). Determine the gate resistance R_G which was used to measure the device switching characteristic from the specifications, and choose R_G to be approximately twice that value to determine the di/dt rate. If the surge voltage is still excessively large, try a different R_G value or add a snubber circuit.

(2.7) Parallel operation

When using IGBTs in a parallel configuration, the collector current temperature coefficient generally has a negative effect so that when channel temperature T_{ch} in one of the devices rises, the gate-to-emitter voltage V_{GE} increases, suppressing the collector. This makes thermal runaway unlikely and prevents current concentration.

However, this only applies to static operation. When the parallel-connected devices are used in a switching application, attention should be paid to the following problems:

- Oscillation phenomenon
- Current imbalance due to differences in V_{GE}(OFF), V_{CE}(sat) and tf
- Current imbalance caused by wiring and other external circuits

① Oscillation phenomenon

When IGBTs are “directly” connected in parallel, the gate-to-emitter voltage causes oscillation, inducing an oscillation collector current.
This oscillation current can cause the device to go out of control or increase the power dissipation. An effective countermeasure is to insert a resistor of several to 10 Ω in series with each gate electrode, as shown in Figure 5.9.11. In the case of modules, since wiring runs directly from the printed circuit board to the electrode leads, care must be taken to ensure that the wiring is not too long and that the inserted resistor is connected as close as possible to the module electrode.

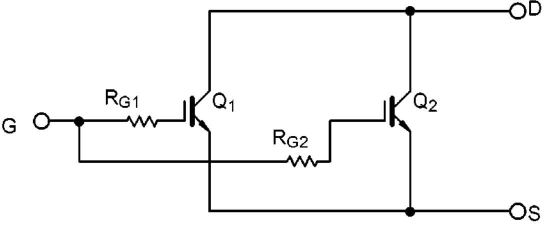


Figure 5.9.11

② Current imbalance due to differences in V_{GE}(OFF), V_{CE}(sat) and tf

When connecting IGBTs that have different V_{GE}(OFF), V_{CE}(sat) and tf values in parallel, be sure to connect the gate electrodes in parallel using the method described in ① above. Since the gate voltages of all parallel-connected IGBTs are the same, if the gain (Yfs) is assumed to be the same, the collector currents will vary from IGBT to IGBT.

Furthermore, if one of the devices has a low V_{GE}(OFF) and more collector current flows in this device, its channel temperature Tch may increase above that of the other devices. This causes the gate-to-emitter voltage to increase and the collector current to decrease with the result that the device is saturated with a current of arbitrary value.

However, if the difference in divided current is large at turn-off time, current concentration occurs (rapidly-increasing current flows in one device), causing the collector-to-emitter voltage change rate dv/dt to be exceeded. Hence it is required that V_{CE}(sat) be approximately equal in all connected devices. For some large-current IGBTs, V_{CE}(sat) ranges for parallel use are given in the datasheets as shown in Table 5.9.1.

Table 5.9.1 V_{CE}(sat) classification

Symbol	V_{CE}(sat) Range
A	2.0 V ~ 2.5 V
B	2.3 V ~ 2.8 V
C	2.6 V ~ 3.1 V
D	2.9 V ~ 3.4 V
E	3.2 V ~ 3.7 V
F	3.5 V ~ 4.0 V

(2.8) Isolation voltage (V_{ISOL})

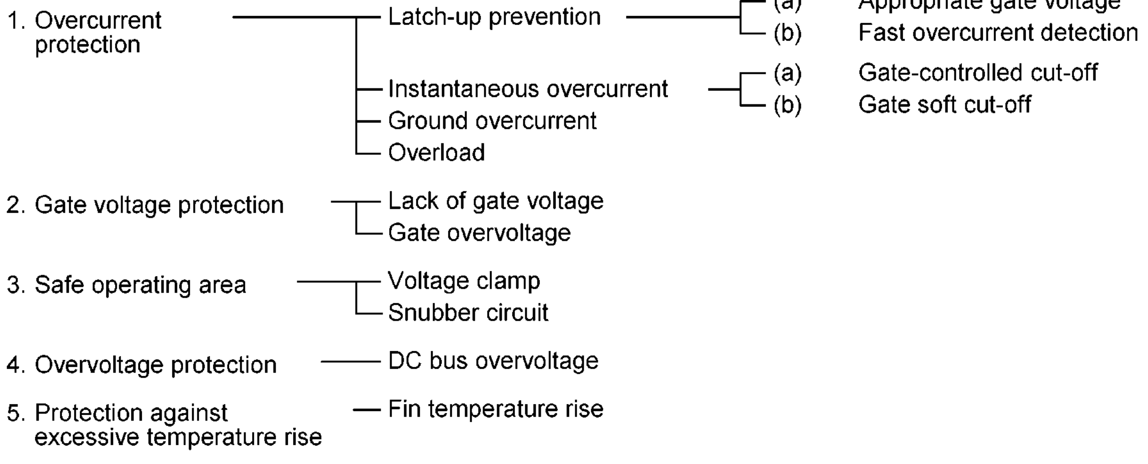
IGBT modules are insulated by a DBC circuit board so that multiple modules can be fitted to a single heat sink. The guaranteed isolation voltage is 2500 V_{AC}; if a higher value is required, consult Toshiba or one of its distributors.

(2.9) Protective measures and circuitry

Table 5.9.2 lists protective measures for IGBTs.

General-purpose IGBTs do not suffer from latch-up as long as the gate voltage is held below the rated value. If this value is exceeded, however, the short-circuit current increases, making protection against latch-up difficult. A stable gate power supply is therefore required.

Table 5.9.2 IGBT protection measures



① Load short-circuit protection

When using transistors in bridge-type inverter circuits, the short-circuit capability of the devices is a very important factor.

Figure 5.9.12 compares the short-circuit capabilities of bipolar junction transistors (BJTs) and IGBTs. For BJTs, the SOA characteristic deteriorates rapidly in the high-voltage regions. Conversely, IGBTs exhibit constant power characteristics, even in the high-voltage regions. Since the short-circuit SOA expands as the pulse width is narrowed, it is desirable in the case of IGBTs to detect and suppress overcurrent quickly (within 10 μs).

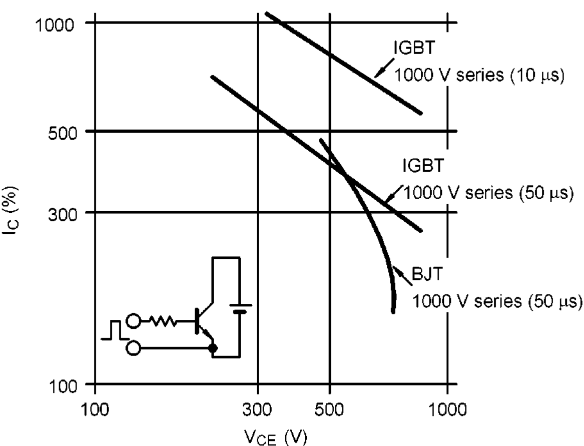


Figure 5.9.12 Short-circuit SOA characteristic

There are essentially four methods for protecting against short-circuit overcurrent.

Figure 5.9.13 shows the first, and simplest, protection method, whereby the gate signal is turned off quickly when an overcurrent level is detected. Good overcurrent-detection and noise-resistance techniques are important for high-speed overcurrent detection. Detection methods using magnetic balancing hole CT as a current sensor, or alternating CT to detect current capacitor discharge are available.

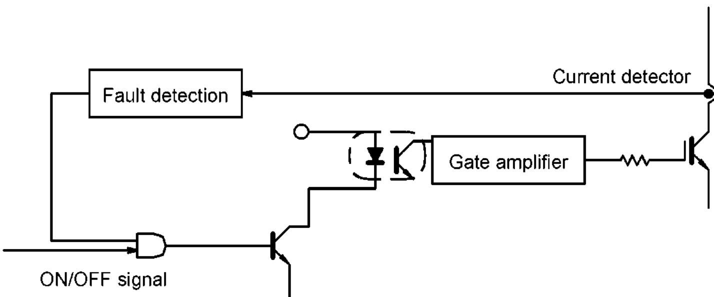


Figure 5.9.13 High-speed overcurrent detection method

A second method is shown in Figure 5.9.14. This is referred to as the test pulse protection method. The gate signal is maintained as long as the load is normal. In the event of an abnormality, the gate signal is shut off and the test pulse is held active.

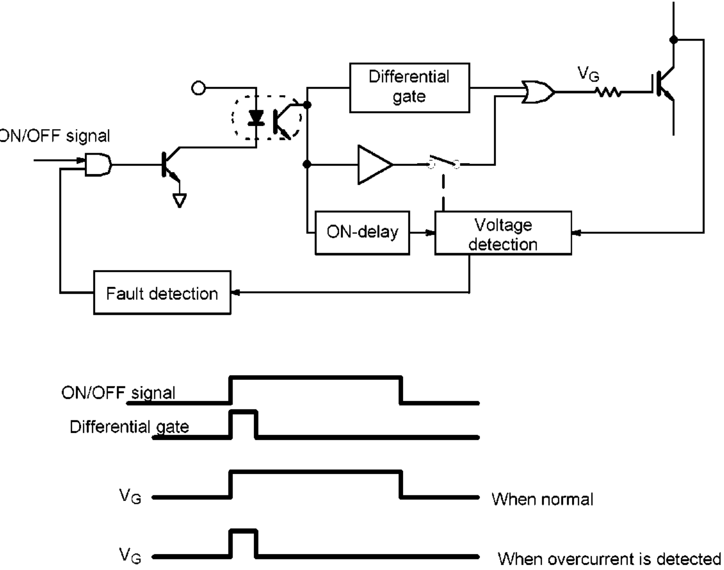


Figure 5.9.14 Test pulse protection method

Figure 5.9.15 shows a third method, referred to as the gate change rate control protection method, in which the circuit is driven by a high-speed ON/OFF signal as long as the load is normal. In the event of overcurrent, the signal is switched to a slow-falling gate voltage so that the faulty current is shut off with a gentle transition to reduce surge voltage due to -Ldi/dt. This allows the protective cut-off to occur within the safe operating area.

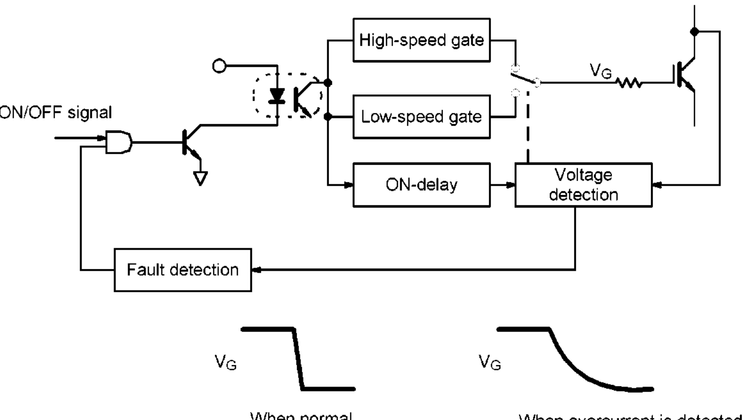
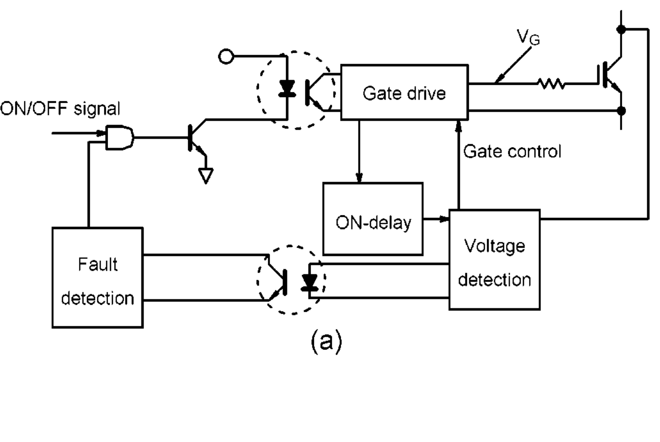


Figure 5.9.15 Gate change rate control protection method

The fourth method, shown in Figure 5.9.16, is referred to as the gate control protection method. When overcurrent is detected, the gate voltage is reduced to limit the faulty current. If the condition persists for a certain amount of time, the gate signal is turned off. This method is resistant to noise and is highly reliable.



50 A / div

VG

5 µs / div

IGBT rating 1000 V, 25 A

(b)

Figure 5.9.16 Gate control protection method

Figure 5.9.17 shows an example in which the short-circuit SOA is increased using the gate control protection method.

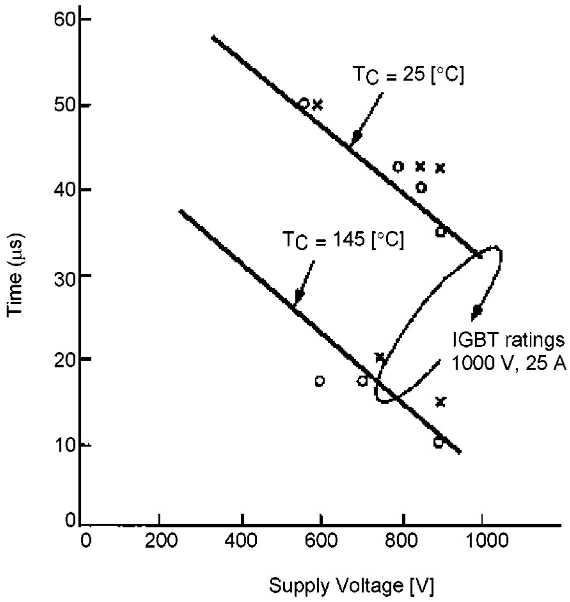


Figure 5.9.17 Expanded short-circuit SOA

② Snubber circuit

The IGBT is an easy-to-use power device due to its large safe operating area. However, its tendency to produce a surge voltage when switched rapidly usually requires that a clamping circuit be used.

Figure 5.9.18 shows typical snubber circuits and their main features. The circuit in (a) is the simplest, consisting of only a single capacitor connected between the DC terminals. It is suitable for 50-Aclass IGBTs.

The circuit in (b) can absorb a large surge energy with a resistance condenser diode (RCD) snubber at high speed via a capacitor. It is suited to medium-capacity converters.

The circuit in (c) has RCD snubbers fitted to each arm so that devices connected in parallel will have a pair of snubbers for every one or two devices. Note that diodes should have fast and soft recovery characteristics. To combat a surge voltages that develop across a diode, connect a ceramic capacitor in parallel to the diode.

The circuits in (d) and (e) have a large snubbing effect but exhibit large power dissipation as well. They are used in applications where the IGBT has a small voltage withstand margin.

Which snubber circuit is most appropriate depends on the main circuit wiring and gate drive methods, since the surge voltage varies according to these methods. Therefore, it is important to understand snubber circuit characteristics, and to determine circuit constants experimentally, before choosing a protective circuit or a combination of protective circuits for an application.

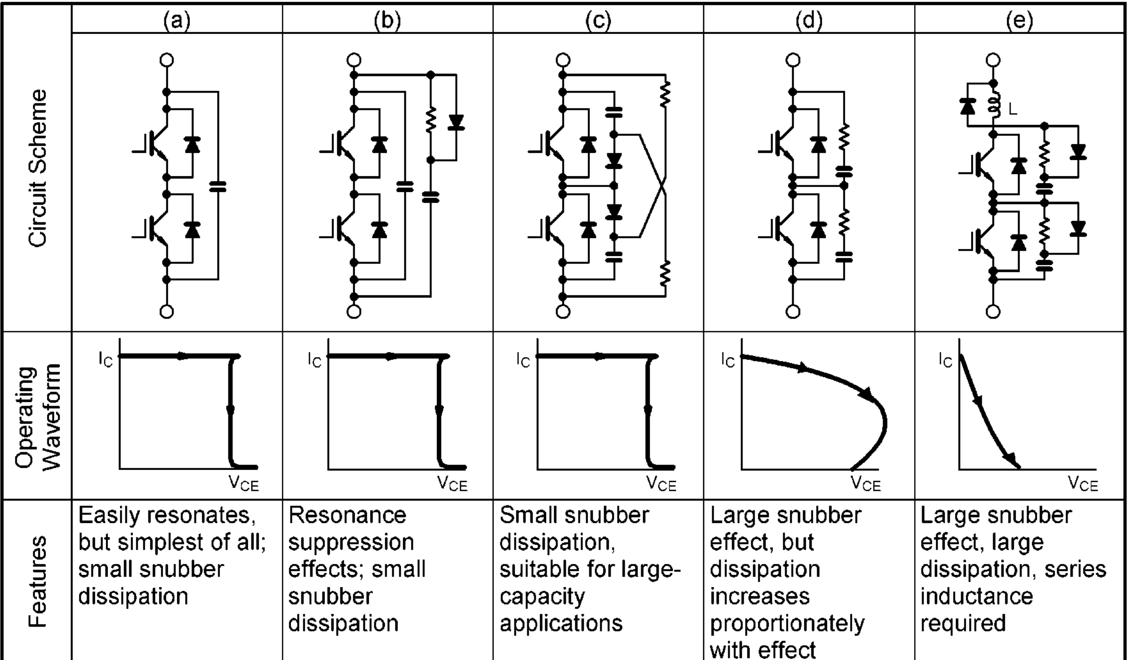


Figure 5.9.18 Snubber circuits and features

③ Temperature protection

Because IGBT modules handle high current, they dissipate a lot of power and therefore require a heat sink for cooling.

To minimize the size of the heat sink, forced air cooling or pipe line cooling must be used. However, if a cooling failure occurs, such as a fan stopping, the device temperature can rise rapidly, leading to breakdown.

To prevent IGBT damage due to a cooling system failure, use a temperature detector, such as a thermistor or thermostat, to shut off the current supply to the load when the temperature is found to be too high. After resolving the problem, operation can be resumed.

(2.10) Mounting precautions (modules)

(1) Soldering

Since the terminals of IGBT modules are usually fastened ontoor screwed into the PCB, soldering is not recommended.
If a wire must be soldered to a fastener terminal, 6/3 solder should normally be used and the soldering operation should be completed within three seconds at 350°C or within ten seconds at 260°C.

(2) Fastener terminals

Fastener terminals are usually provided for the gate and emitter terminals. Receptacles that adhere to accepted standards should be used to avoid imparting stress to the terminals.

(3) Screw terminals

When tightening screw terminals, be careful not to apply too much torque, as too much torque can wrench off the screw or overstress the casing.

Also, the contact thermal resistance can become saturated if the specified torque is exceeded. To avoid these problems, use the recommended tightening torques listed in Table 5.9.3.

Table 5.9.3 Recommended tightening torque

Screw or Bolt	Torque	(Maximum)
M4 × 0.7	1.0 N•m ~ 1.4 N•m	2 N•m
M5 × 0.8	2.0 N•m ~ 2.5 N•m	3 N•m
M6 × 1.0	2.6 N•m ~ 3.0 N•m	3 N•m

(4) Bends in terminals

The copper electrode fastener terminals of IGBT modules are fabricated by bending. Excessive stress or repeated bending can break them.

To prevent this, use a busbar and insert a fixed terminal when making external connections.

When connecting wiring, be careful not to apply excessive force to the fastener terminals.

(5) Heat radiation lubricant

YG6260 heat radiation lubricant from Toshiba Silicone is recommended for semiconductor devices.

Apply a thin, even (100 μm ~ 200 μm) coating of lubricant.

The heat radiating plane of IGBT modules is already insulated, so there is no need to use an insulating type of heat radiation lubricant. S-200 from Nikkei Jointal is adequate.

(6) Flatness and contact thermal resistance

The flatness of IGBT modules is within ±120 μm for two-hole products and ±150 μm for four-hole products. The average flatness is negative (that is, the surface is concave). Contact thermal resistance versus flatness for products with concave surfaces is shown in Figure 5.9.19 and 5.9.20.

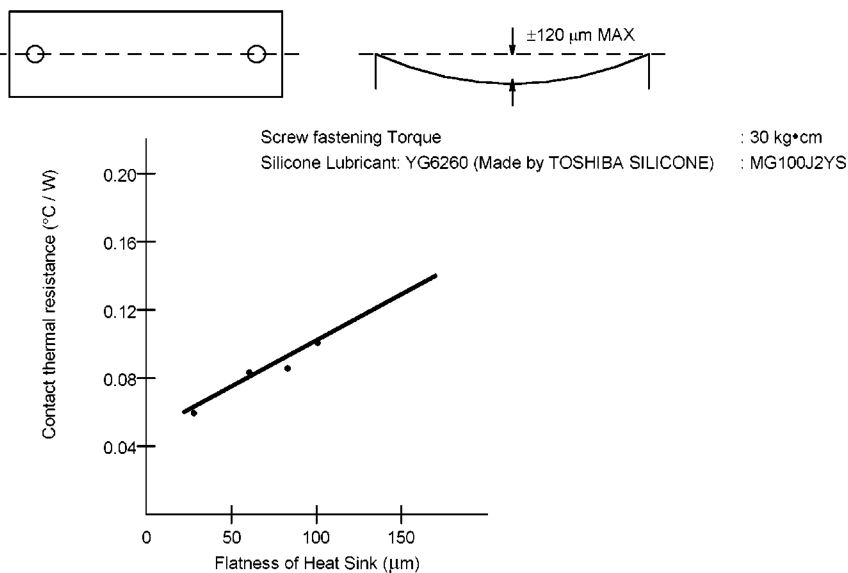


Figure 5.9.19 Relationship between flatness of heat sink and contact thermal resistance (for two-hole mounting)

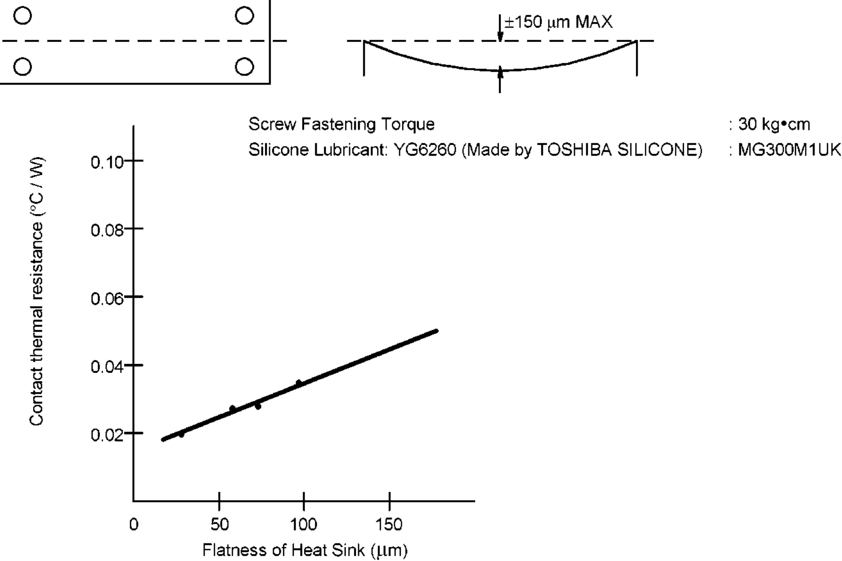


Figure 5.9.20 Relationship between flatness of heat sink and contact thermal resistance (for four-hole mounting)

The contact thermal resistance increases when the surface is excessively concave. This is because the air gap between the heat sink and the device degrades the heat radiation effect.

(7) Attaching an IGBT to a heat sink

① Make sure that the heat radiation surface os the IGBT and the contact surface of the heat sink are both clean and free of foreign matter.

② Apply a coating of radiation compound to the IGBT heat radiation plane, as shown in Figure 5.9.21(a).

③ Place the IGBT on the heat sink. Press on it with your hand to spread out the compound and to purge any air between the IGBT and the heat sink, as shown in Figure 5.9.21 (b).

④ Following the sequence shown in Figure 5.9.21(c), use a manual or motor-driven screwdriver to lightly tighten the four screws to the recommended torque of 0.4 N•m ~ 0.9 N•m. Do not use an air-driven screwdriver as this will make it difficult to control the fastening torque.

⑤ Firmly tighten the screws in the order shown in Figure 5.9.21(d) to a torque of 2.0 N•m, using a manual or motor-driven screwdriver.

⑥ Wipe off excess radiation compound seeping out from between the module and heat sink as shown in Figure 5.9.21(e). If there is only a small amount of excess compound seeping out from between the devices, then the amount of compound used was probably insufficient. In this case, detach the module, add more compound and then reattach it.

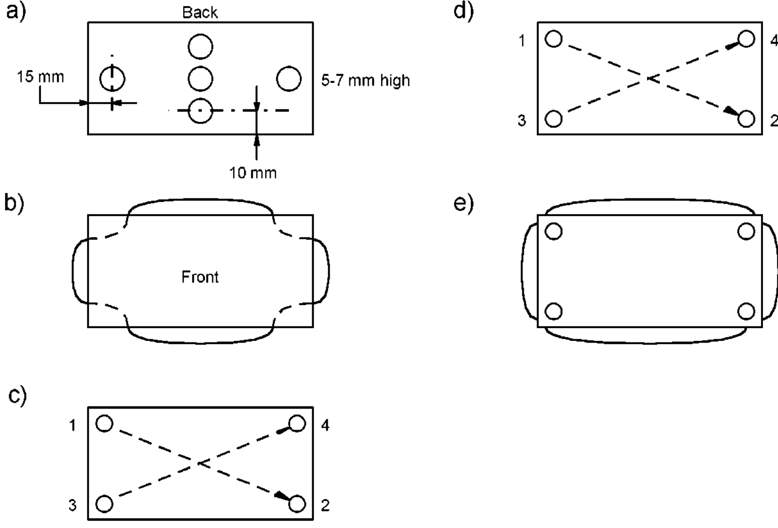


Figure 5.9.21 Procedure for attaching an IGBT to a heat sink

(8) Dropping

The DBC board of an IGBT module is ceramic (Al_2O_3 or AlN) and can be cracked or damaged by the impact if it is dropped. This is especially true for high-current IGBTs because of their heaviness. When handling unpacked, single-IGBT modules, be careful not to drop them. Packaged modules can be handled in the same way as other products.

(9) ESD (electrostatic discharge)

IGBTs have a gate structure similar to that of MOSFETs. Full antistatic measures should be taken to protect them.

5.9.3 Reliability Characteristics

(1) Reliability test results

As an example, Table 5.9.4 lists the results of reliability tests performed on a MODULE-type IGBT. Table 5.9.5 lists failure criteria applied during the tests.

A basic method frequently used to evaluate reliability is to have a device in operation and to perform a detailed analysis of changes that occur in characteristics over time. As an example, Figures 5.9.22 to 5.9.26 show changes in characteristics that occurred during the lifetime tests described in Table 5.9.4.

Test results indicate that, although the device was operated as its absolute maximum ratings, the initial characteristics remained stable over a long period of time.

Consequently, this device can be expected to offer high reliability in an actual application.

Table 5.9.4 Reliability test results for the MG400Q1US1 IGBT

	Test	Applicable Standard JIS C7021	Test Conditions	No. Of Devices Test	No. Of Failures
Lifetime Tests	Steady-state operation	B-6	Δ Tc = 60°C, ON for 5 mins, off for 7 mins Ta = 25°C, 1,000 hrs	36	0
	High-temperature reverse bias	B-8	Tc = 125°C, V_{GE} = 20 V 1,000 hrs	36	0
	High-temperature storage	B-10	Ta = 125°C, 1,000 hrs	30	0
	High-temperature, high Humidity storage	B-11	Ta = 60°C, RH = 90% 1,000 hrs	30	0
Environment Tests	Temperature cycling	A-4	–40°C ~ 25°C ~ 125°C ~ 25°C 10 cycles	50	0
	Moisture resistance	A-5	Ta = ~ 65°C, RH = 90 ~ 98% 10 cycles	36	0
Mechanical Tests	Vibration	A-10	100 ~ 2,000 Hz, 196 m/s^2 4 times each in 3 directions	10	0
	Mechanical shock	A-7	1 ms, 4,900 m/s^2 3 times each in 4 directions	10	0
	Constant acceleration	A-9	49,000 m/s^2 1 minute each in 6 directions	10	0
	Lead integrity	A-11	Fastening torque 3.0 N•m Once for 5 secs	10	0

Table 5.9.5 Failure Criteria for the MG400Q1US1 IGBT

Parameter	Symbol	Measuring Conditions (Ta=25°C)	Criteria	
			minimum	maximum
Gate leakage current	I_{GES}	V_{GE} = ±20 V, I_E = 0	—	USL × 2
Collector cut-off current	I_{CES}	V_{CE} = 1200, V_{GE} = 0	—	USL × 2
Drain-to-emitter cut-off voltage	$V_{GE}(OFF)$	V_{CE} = 5 V, I_C = 400 mA	LSL × 0.8	USL × 1.2
Collector-to-emitter saturation voltage	$V_{CE}(sat)$	I_C = 400 A, V_{GE} = 15 V	—	USL × 1.2

USL: Upper specification limit; LSL: Lower specification limit

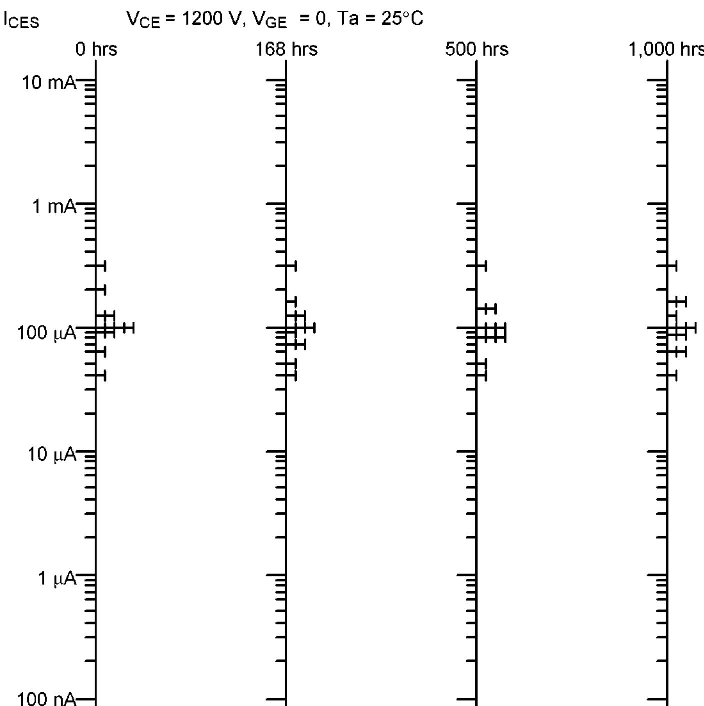


Figure 5.9.22 I_{CES} results from steady-state operation lifetime test for the MG400Q1US1 IGBT

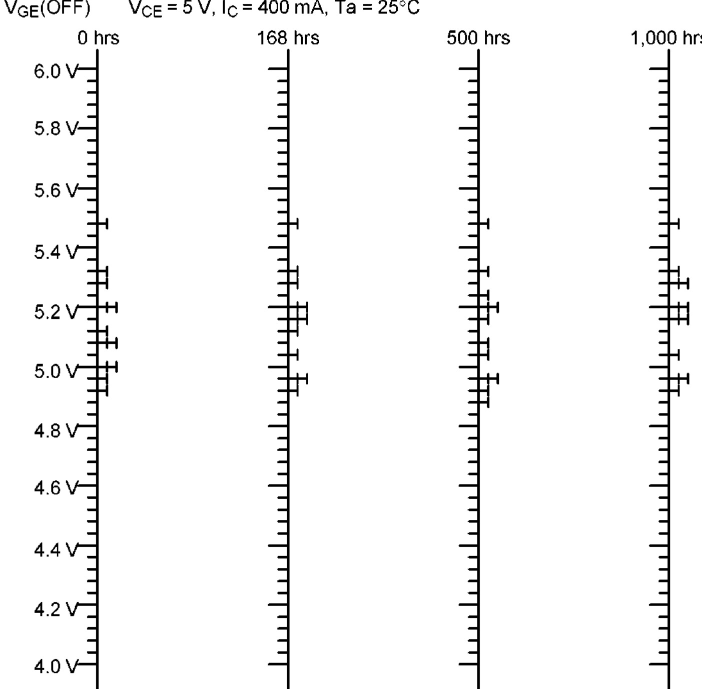


Figure 5.9.23 V_{GE}(OFF) results from steady-state operation lifetime test for the MG400Q1US1 IGBT

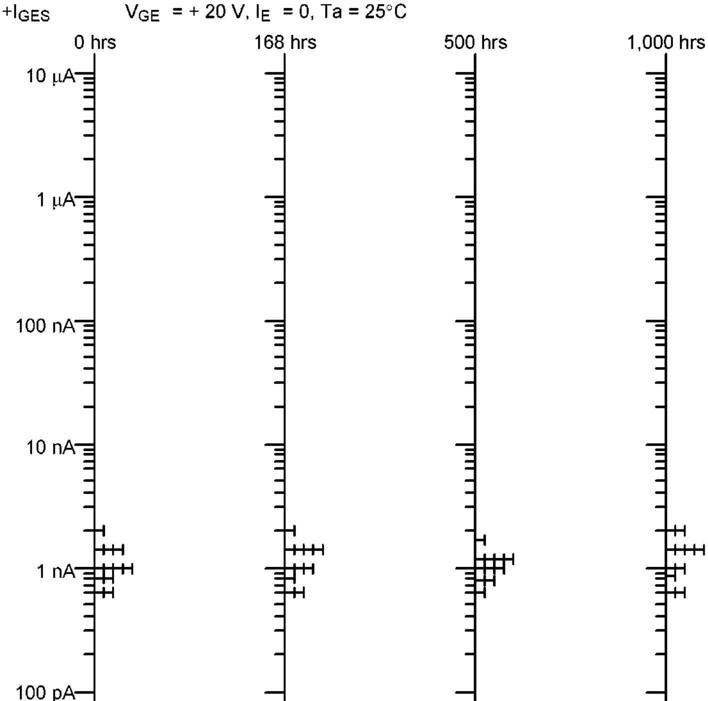


Figure 5.9.24 $+I_{GES}$ results from steady-state operation lifetime test for the MG400Q1US1 IGBT

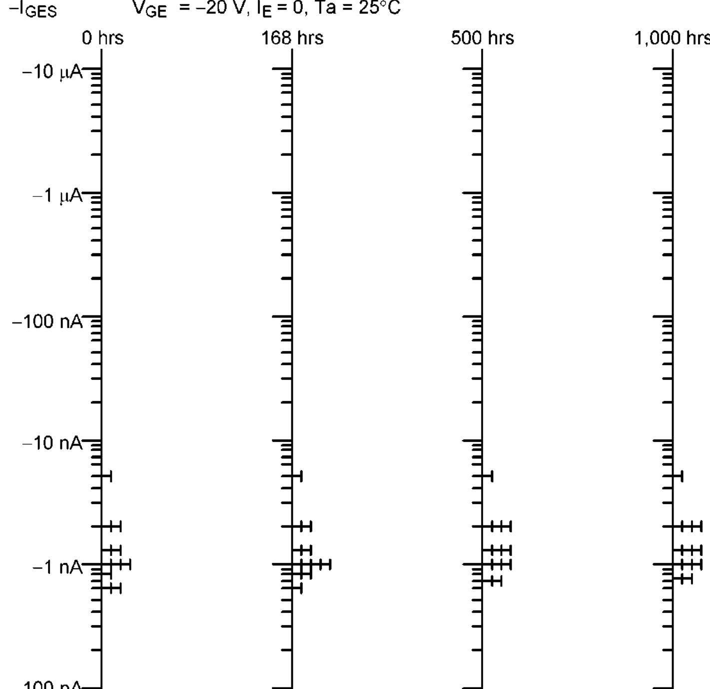


Figure 5.9.25 $-I_{GES}$ results from steady-state operation lifetime test for the MG400Q1US1 IGBT

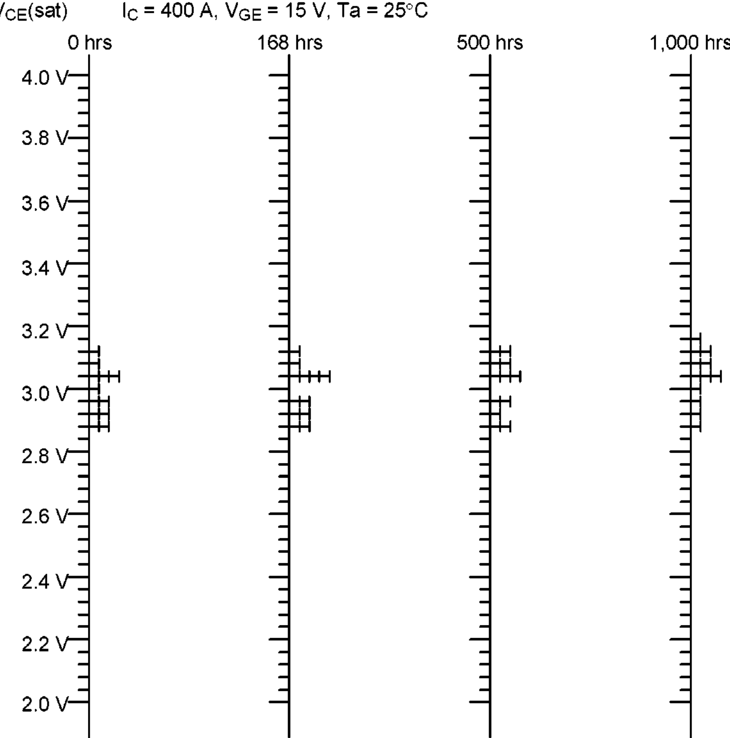


Figure 5.9.26 V_{CE}(sat) results from steady-state operation lifetime test for the MG400Q1US1 IGBT

(2) Reliability characteristics

Power cycles

IGBTs are sometimes used in numerically controlled motor control whereby devices are subjected to rapid changes in junction temperature while case temperatures remain almost constant.

Figure 5.9.27 shows limits on the number of power cycles in relation to changes in the junction temperature. An IGBT lifetime of only 2.5×10^4 at ΔT_j = 100°C jumps to 3×10^5 when the device is operated at ΔT_j = 50°C. In other words, the lifetime increases almost ten-fold when the temperature is reduced by 50°C.

This suggests that ΔT_j should be reduced as much as possible when designing a circuit.

The failure mode for repeated power cycling is "bonding wire open".

When IGBTs are used for motor control in applications such as pump blowers, changes in case temperatures occur, but usually very slowly (since typically poewr cycling occures only once a day).

To evaluate device tolerance to temperature changes in this type of application, try reduce the frequency of power cycling while varying the case temperature. Toshiba verifies device reliability by performing the intermittent operation tests listed in Table 5.9.4.

In the examples in Figures 5.9.22 ro 5.9.26, the MG400Q1US1 was evaluated for 5000 cycles at ΔTc = 60°C. Assuming one cycle per day, this works out to a reliable lifetime of more than ten years.

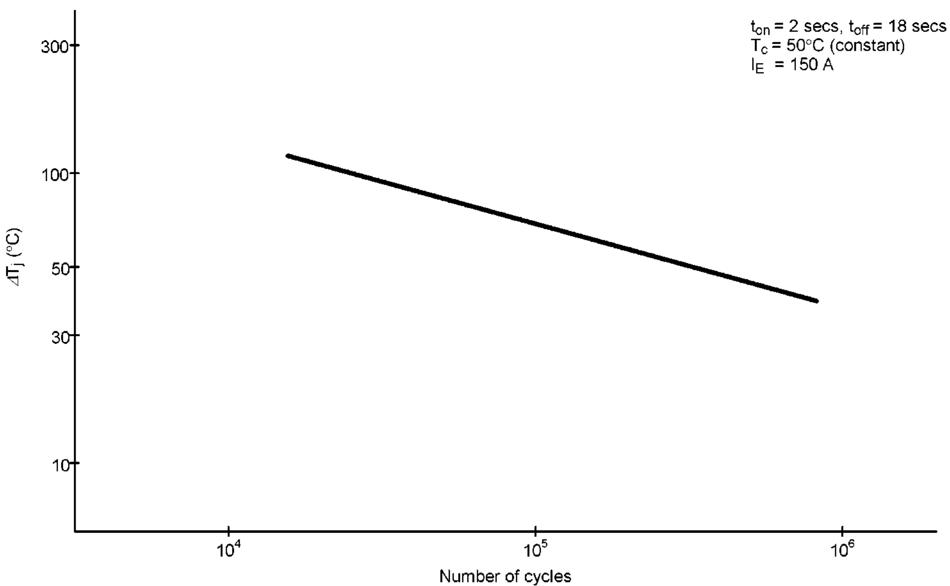


Figure 5.9.27 Example of power cycle lifetime characteristic for MG150Q2YS1

5.10 Rectifier and Thyristor Reliability

5.10.1 Overview

(1) Features

Rectifiers

The term rectifier generally refers to rectifier diodes, but can also include constant-voltage (zener) diodes.

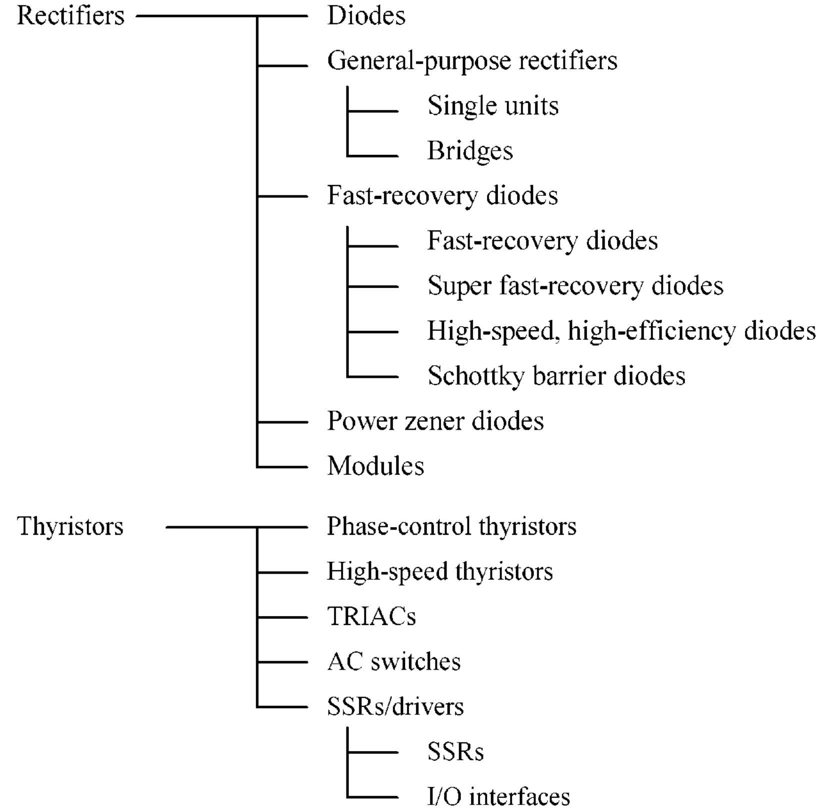
Thyristors

This is a type of rectifier that is normally off (i.e. does not pass current), but turns on when a trigger signal is applied to the gate.

SSRs

These semiconductor switching circuits take advantage of the gate-controlling property of thyristors.

The above are broad classifications. Devices in these categories can be further classified according to differences in characteristics as follows:



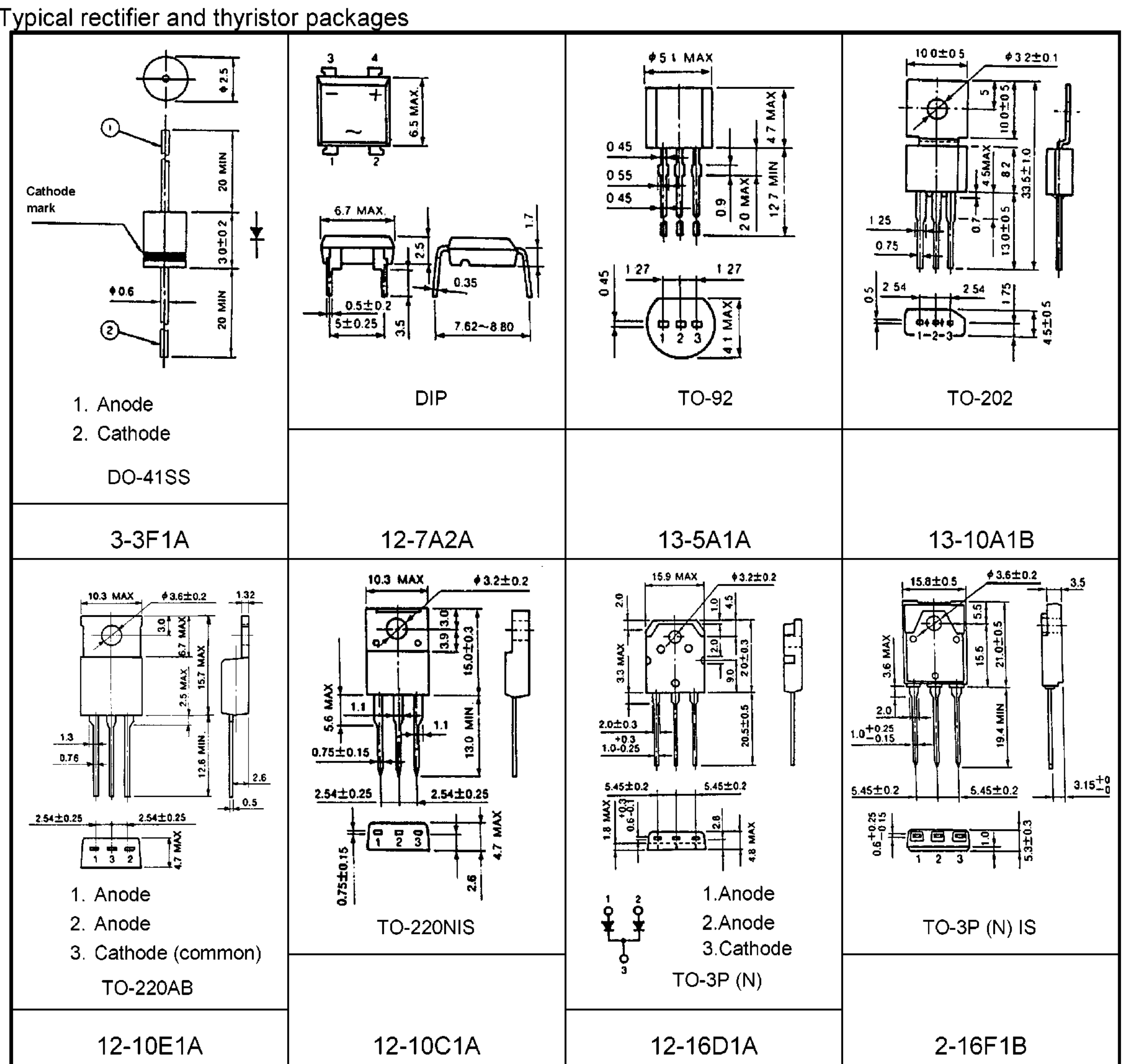
(2) Packages

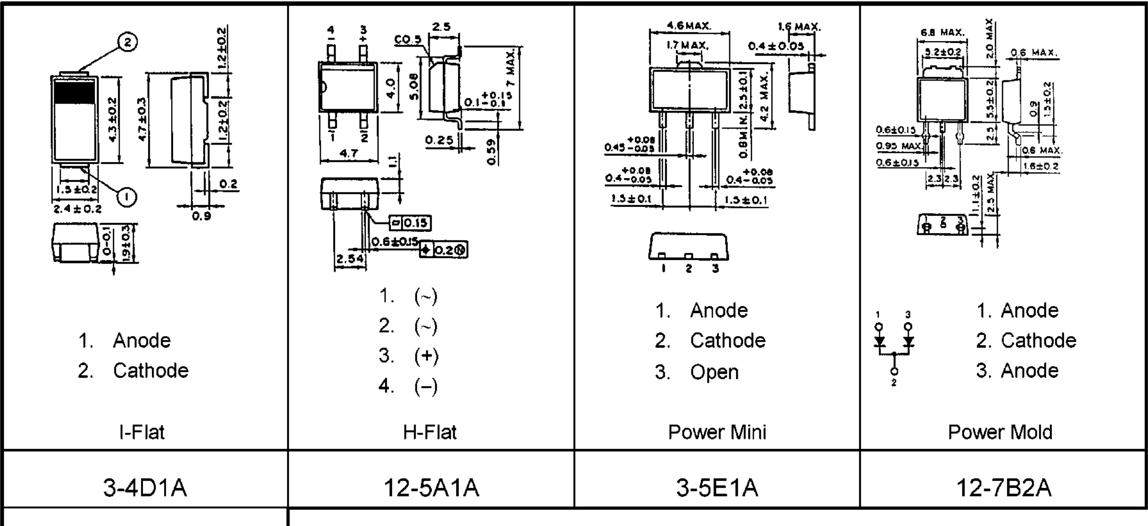
Table 5.10.1 lists typical packages classified by device type.

Table 5.10.1 Typical packages classified by device type

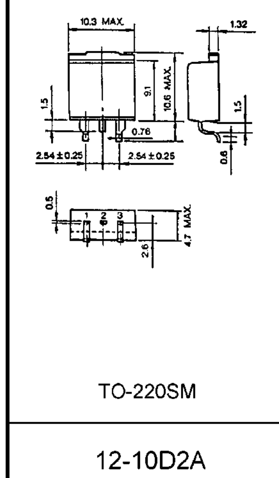
Classification		Package	Typical Products
Plastic mold		DO-41SS	S5688G, 1ZB6.8, 05NU42, 1DL42, 1GWJ43
		DO-15L	1R5GZ41, 2Z12, TVR4N, 1R5GU41
		DO-201AD	3GZ41, 3JH41, 2NU41, 3JU41, 3DL41, 3GWJ42
		DIP	1J4B42, SM6J44
		TO-92	SF0R1G42, SF0R3J42, RSF05G1-1P, SM1G43
		TO-202	SF2J41, SM2G41
		TO-220AB	SF8J41A, SM8J45
		TO-220NIS	5DL2CZ47A, 5GWJ2CZ47, SF8JZ47, SM8JZ47
		TO-3P (N)	20DL2C41A, 16GWJ2C42
		TO-3P (N) IS	SF25JZ51, SM25JZ51
	Surface-mount	I-Flat	U1GC44, U1BZ12, U05JH44, U1JU44, U1GWJ44
		H-Flat	U05J4B48
		Power-Mini	U1GWJ2C42, URSF05G49-1P
		Power-Mold	U2GWJ2C42, U3GWJ2C42
		TO-220SM	USF8J48, USM8J48

Typical rectifier and thyristor packages





1. Anode 2. Cathode	1. (~) 2. (~) 3. (+) 4. (−)	1. Anode 2. Cathode 3. Open	1. Anode 2. Cathode 3. Anode
I-Flat	H-Flat	Power Mini	Power Mold
3-4D1A	12-5A1A	3-5E1A	12-7B2A



TO-220SM
12-10D2A

(3) Structure

Figure 5.10.1 shows the structure of a device, using the DO-41SS as an example.

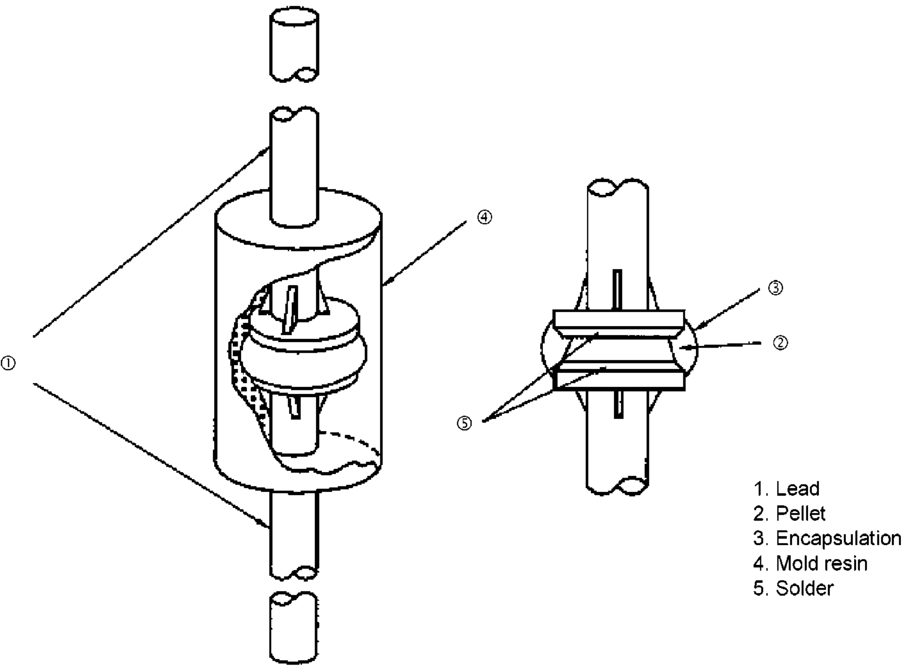


Figure 5.10.1 Internal structure of DO-41SS

This structure includes a pellet ② affixed to lead ① using solder ⑤.

The encapsulation ③ and mold resin ④ protect the pellet against external forces, thermal stress and chemicals, in order to help maintain stable device characteristics.

5.10.2 Design Precautions

(1) Absolute maximum ratings

Definition of absolute maximum ratings

Maximum permissible values for current, voltage, reverse voltage and power dissipation in devices (diodes, rectifiers, thyristors and triacs) are stipulated as absolute maximum ratings.

When designing application circuits using semiconductors, a good understanding of absolute maximum ratings is important to ensure that the devices operate efficiently and reliably.

Semiconductor devices are unique in that their electrical characteristics are extremely sensitive to temperature. Absolute maximum ratings are specified in order to guard against problems which could arise as a result of device temperature sensitivity.

To guarantee a useful lifetime and the reliability of a device, no absolute maximum rating must ever be exceeded, even momentarily. These values are specified according to the material, design and manufacturing conditions of the device type and package.

Table 5.10.2 lists sample absolute maximum ratings.

Table 5.10.2 Sample maximum ratings

Parameter		Symbol	Rating	Unit
Repetitive peak OFF-state voltage	SF8GZ47	V_{DRM}	400	V
Repetitive peak reverse voltage	SF8JZ47	V_{RRM}	600	
Non-repetitive peak OFF-state voltage	SF8GZ47	V_{RSM}	500	V
Reverse Voltage (without repetition, <5 ms, T_j = 0 ~ 125°C)	SF8JZ47		720	
Average ON-state current (Half Sinewave, Tc = 72°C)		$I_T(AV)$	8	A
RMS ON-state current		$I_T(RMS)$	12.6	A
Peak 1-cycle surge ON-state current		I_{TSM}	120 (50 Hz)	A
I^2t Limit		I^2t	72	A^2s
Critical rate of rise of ON-state current (Note 1)		di/dt	100	A / µs
Peak gate power dissipation		P_{GM}	5	W
Average gate power dissipation		$P_G(AV)$	0.5	W
Peak forward gate voltage		V_{FGM}	10	V
Peak reverse gate voltage		V_{RGM}	–5	V
Peak forward gate current		I_{GM}	2	A
Junction temperature		T_j	–40 ~ 125	°C
Storage temperature		T_{stg}	–40 ~ 150	°C
Isolation voltage (AC 60 secs)		V_{ISOL}	1500	V

Rated voltage of rectifiers

Select devices with a rated voltage 1.5 to 2 times the tolerable peak reverse voltage per device, taking into account power supply fluctuations, transformer regulation and switching surges.

In general, for 100-VAC lines, Toshiba recommend that devices be able to withstand 400 V; for 200 VAC lines, the devices should be able to withstand 600 V.

Excessive reverse voltage due to surges from external sources or load circuits can result in excessive reverse power dissipation in the avalanche region, causing the device to degrade or break down. In such cases, a surge-absorption circuit must be added for protection.

Rated current of rectifiers

The rated current of a rectifier is stipulated as the average value of a 180° half-sine waveform. This is the maximum current that can be supplied to the device under the specified conditions without exceeding the maximum junction temperature T_j(max).

The current which actually flows in a device is determined by the load conditions (steady-state current and transient current) and the cooling conditions.

For capacitive loads, the conduction angle of the device is narrow in comparison with the angles for resistive and inductive loads.

It should be noted that, even for the same average current value, the peak current in a capacitive load can become considerably larger than that in a resistive load, resulting in an effective current that is larger than the rated value.

Also, with capacitive loads, transient currents of up to 10 times the peak value of the steady-state current can occur when the power supply shuts the circuit off. For this reason, choose devices that are rated for a large surge current. Particularly in applications where a device is repeatedly turned on and off, the expected increase in junction temperature (ΔT_j) must be estimated from the I_F-v_F and r_{th}(j-c)-t characteristics, so as to ensure that the temperature remains below T_j(max).

Surge forward current

When a surge forward current flows, the junction temperature momentarily exceeds T_j(max). This rating is stipulated to account for abnormal currents which occur less than 100 times during the life of the device.

It therefore does not apply to motor lock current or in-rush current at power-on.

Junction temperature

The maximum junction temperature T_j(max) is determined by the materials used to fabricate the device and their reliability. This parameter must be considered in relation to reliability factors such as degradation and lifetime, not simply in relation to operability of the device. Device degradation is generally accelerated as the junction temperature increases. Mean lifetime Lm (hours) and junction temperature T_j (K) are known to have the following relationship (where A and B are device constants):

$$\log Lm = A + \frac{B}{T_j} \quad \cdots\cdots\cdots\cdots (2\text{-}2)$$

Note also that the reverse current increases with temperature. A vicious circle can result whereby increased reverse current increases the power dissipation, which in turn increases the junction temperature, which in turn further increases the reverse current, and so on leading to thermal runaway in the device. For this and other reasons, the junction temperature and heat-radiating conditions of devices must be considered carefully when circuits are being designed.

Storage temperature

The storage temperature T_{stg} refers to the ambient temperature range in which a device can be safely stored when not in operation. It is specified according to the characteristics and reliability of the device's constituent materials (other than those of the silicon chip). When storing devices, take precautions against lead oxidation and other related problems.

(2) Design precautions

When designing rectifier and thyristor circuits, the first priority is to ensure that the absolute maximum ratings are not exceeded. Decapsulation analysis of products returned to Toshiba reveals that in almost every case faults are caused by surges which exceed the rated current values.

To counter this, be sure to derate the devices in your design sufficiently, after carefully considering the absolute maximum ratings and the reliability characteristics (described later).

Junction temperature

The junction temperature rating of a device is just as important as the rated voltage and the rated current.

To control the junction temperature, the power dissipation of the device must be limited and sufficient heat radiation for the device and circuit board must be provided.

Protection against overcurrent

If protection is not provided against overcurrent in circuits which use semiconductor devices, not only can the devices break down, but arcs can also be generated in open devices. The induced magnetic fields often cause mechanical damage.

Overcurrent can result from device faults, commutation failures and short-circuited loads.

Broadly classified, there are two methods of protection against overcurrent. One is to shut off the current with a fuse or by some other means. The other is to limit the current using a reactor or a resistor.

Protection against overvoltage

When selecting devices for applications, designers usually derate the specified OFF-state and reverse voltage ratings by the following safety margins:

Industrial use	By 2.5 ~ 3.5 times
Less critical applications	By 1.4 ~ 2 times

However, this applies to steady-state operation and does not take into account transient voltages generated by various factors. Usually, a protective circuit must be inserted to suppress unwanted voltages.

It is important to know the causes of these unwanted voltages and to take protective measures against them in order to ensure that the above safety factors will be effective.

Protection against dv/dt

The dv/dt rate relates to thyristors. When a fast-rising voltage is applied to a thyristor by the main circuit, it can turn the thyristor on even when no trigger signal has been input to the gate. When it occurs during commutation by a parallel-connected snubber circuit, this dv/dt-ON phenomenon can be effectively suppressed by connecting the snubber circuit and the anode reactor together. Figure 5.10.2 shows an example of this type of limiting circuit.

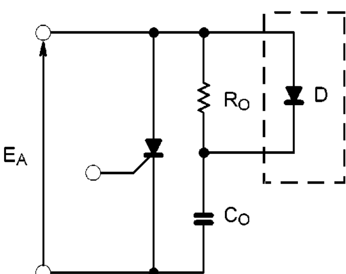


Figure 5.10.2 Example of dv/dt-limiting circuit

Protection against di/dt

The di/dt rate is also relevant to thyristors. It is the critical rate of rise of the ON-state current and is normally rated at 100 A/μs for thyristors and 50 A/μs for triacs. (For more information, refer to the technical data for the device in question.)

The di/dt rate should generally be suppressed to less than 20 or 30 A/μs.

The di/dt tolerance of a device depends on its peak ON-state current, the anode voltage immediately before power-on, the case temperature and gate drive conditions.

If the rated di/dt is exceeded, the device can malfunction or break down. To prevent this, suppress di/dt using an air-core reactor or saturable reactor.

(3) Device-mounting precautions

Using inappropriate methods to mount semiconductors can subject them to thermal and mechanical stresses, degrading their electrical characteristics and reliability.

The following precautions for each package type should be taken when mounting devices on circuit boards:

Lead-forming and molded devices

Do not apply excessive stress to the electrode leads; otherwise, the device may be damaged.

Make sure that no more than 10 N of force is applied to the leads.

When forming the leads, use radio pliers or other appropriate tools so that stress is not applied to the device itself. Also, avoid bending the leads repeatedly. Standard forming tools are available from Toshiba.

When fitting a device to a heat sink, make sure that the heat sink has a smooth surface. Apply a coating of silicone lubricant to the heat sink. Make sure hole diameters closely match screw diameters, and that screws are tightened using the appropriate torque.

Also, ensure that the surface of the heat sink which will come into contact with the device is flat and free of burrs and contaminants.

Surface-mount devices

Refer to Precautions on board mounting and cleaning in Section 3.5.

(4) References

- Toshiba Semiconductor Databook: Rectifiers
- Toshiba Semiconductor Databook: Small and Medium Thyristors
- Toshiba Semiconductor Databook: High-Power Semiconductor Devices (Thyristors, Diodes and IGBTs)
- Toshiba Semiconductor Databook: Small-Signal Diodes
- Toshiba Semiconductor Databook: Small-Signal Transistors (SMDs)

5.10.3 Reliability Characteristics

(1) Reliability test results

As an example, Table 5.10.3 shows the results of reliability tests performed on an S5688G silicon diffused-type rectifier. Table 5.10.4 lists failure criteria applied during the tests.

A basic method frequently used to evaluate reliability is to have a device in operation and to perform a detailed anlaysis of the changes which occur in its characteristics over time. As an example, Figure 5.10.3 shows changes in characteristics which occurred during the lifetime tests described in Table 5.10.3.

Test results indicate that, although the device was operated as its absolute maximum ratings, the initial characteristics remained stable over a long period of time. Consequently, this device can be expected to offer high reliability in an actual application.

Table 5.10.3 Reliability test results for a S5688G silicon diffused-type rectifier

	Test	Applicable JIS C7021 Standard	Test Conditions	No. Of Debices Tested	No. Of Failures
Lifetiem Tests	Steady-state operation	B-13	$T_{F\ (AV)}$ = 1 A, V_{RRM} = 400 V Ta = 25°C, 1,000 hrs	30	0
	High-temperature reverse bias	B-19	Ta = 100°C, V_{RRM} = 400 V, 1,000 hrs	30	0
	High-temperature storage	B-10	Ta = 150°C, 1,000 hrs	30	0
	High-temperature, high-humidity storage	B-11	Ta = 60°C, RH = 90% 1,000 hrs	30	0
Environment Test	Soldering heat	A-1	260°C, 10 secs, once (immersed 1.5 mm from device base)	32	0
	Temperature cycling	A-4	–55°C ~ 25°C ~ 150°C ~ 25°C 100 cycles	50	0
	Thermal shock	A-3	100°C ~ 0°C, 50 cycles	32	0
	Moisture resistance	A-5	Ta = ~ 65°C, RH = 90% ~ 98% 10 cycles	32	0
Mechanical Tests	Vibration	A-10	100 Hz ~ 2,000 Hz, 196 m/s^2 4 times each in 3 directions	11	0
	Mechanical shock	A-7	0.5 ms, 14,700 m/s^2 3 times each in 4 directions	11	0
	Constant acceleration	A-9	196,000 m/s^2 1 minute each in 6 directions	11	0
	Lead integrity	A-11	5.0 N, bent 90° 3 times	11	0
	Drop	A-8	75 cm, on maple board, 3 times	11	0
	Solderability	A-2	230°C, 5 seconds (using designated flux)	11	0

Table 5.10.4 Failure criteria for S5688G

Failure criteria (Ta = 25°C)

Parameter	Symbol	Measuring Conditions (Ta = 25°C)	Criteria	
			minimum	maximum
Peak forward voltage	V_{FM}	I_{FM} = 1.0 A	—	USL × 1.2
Peak repetitive reverse current	I_{RRM}	V_{RRM} = 400 V	—	USL × 2

USL: Upper specification limit; LSL: Lower specification limit

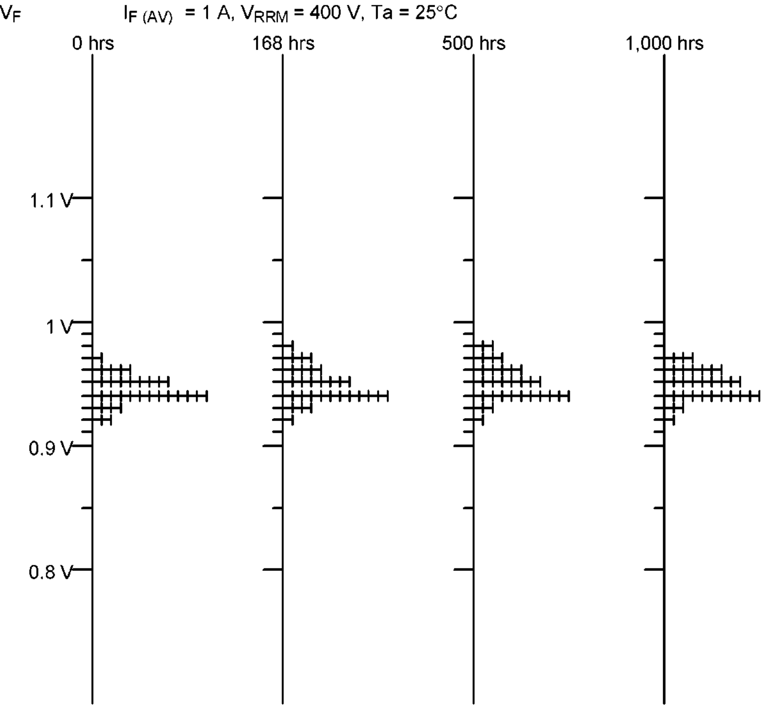


Figure 5.10.3 Results of steady-state operation lifetime test for the S5688G silicon diffused-type rectifier