■ OVERVIEW

The PLL0305A is a PLL synthesizer LSI fabricated using NPC's original molybdenum-gate CMOS technology. The input frequency divider ratio can be set by externally inputting serial data. The reference frequency divider ratio can be selected from 8 choices stored in the built-in ROM.

■ FEATURES

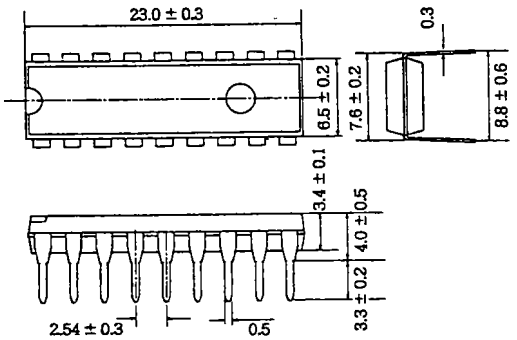
- 30 MHz (5 V, F_{IN})
- 15 MHz (5 V, X_{IN})
- Reference frequency divider ratios 16, 512, 1024, 2048, 3668, 4096, 6144, 8192
- Input frequency divider ratios 5 to 16383
- Lock detector pin
- Can be used with active or passive filters

■ APPLICATIONS

- Scanning receivers
- Amateur radios
- Radios
- Other

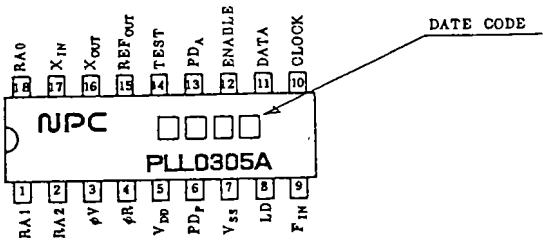
■ PACKAGE DIMENSIONS

Unit: mm

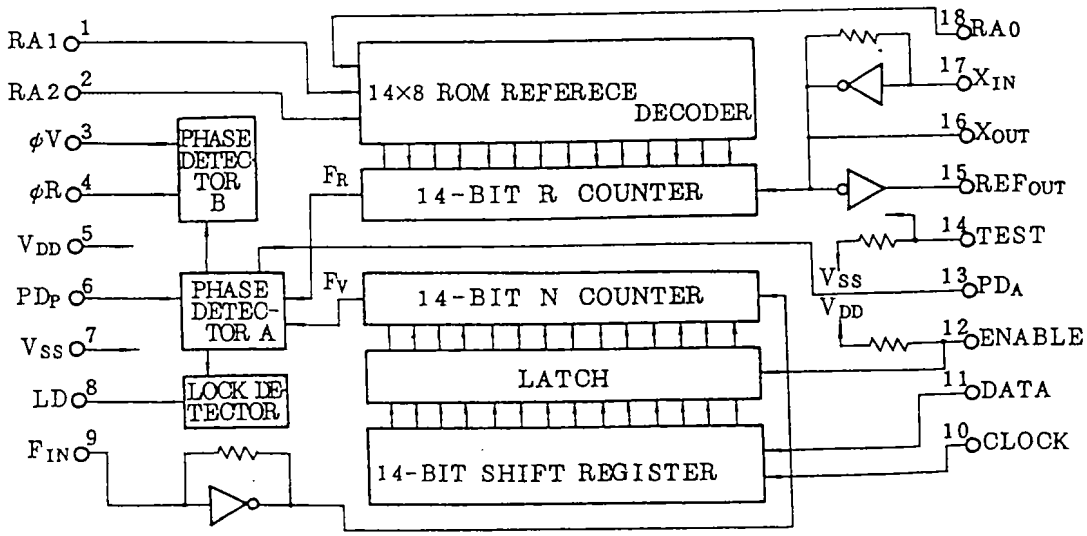


■ PINOUT

TOP VIEW



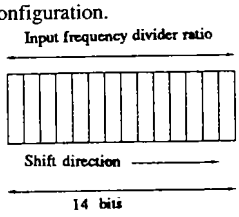
■ BLOCK DIAGRAM



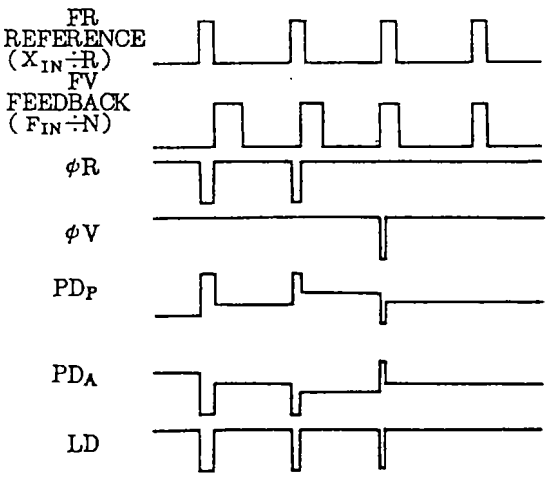
■ PIN DESCRIPTION

NAME (No.)	DESCRIPTION
RA0 (18) RA1 (1) RA2 (2)	Input pins used to select the reference frequency divider ratio from the table.
øV (3) øR (4) PDP (6) PDA (13)	Outputs for a lowpass filter. PDP and PDA are single-ended, tristate outputs. Connect the filter in use to the corresponding output pin. PDP .... passive filter PDA .... active filter øV, øR .... differential filter
VDD (5)	Power supply 4.5 to 5.5 V
VSS (7)	Ground
LD (8)	Unlock detection. When unlocked, it is "L." When locked, it is "H."
FIN (9)	Input frequency divider (N COUNTER) input. Internal feedback resistor for AC coupling.

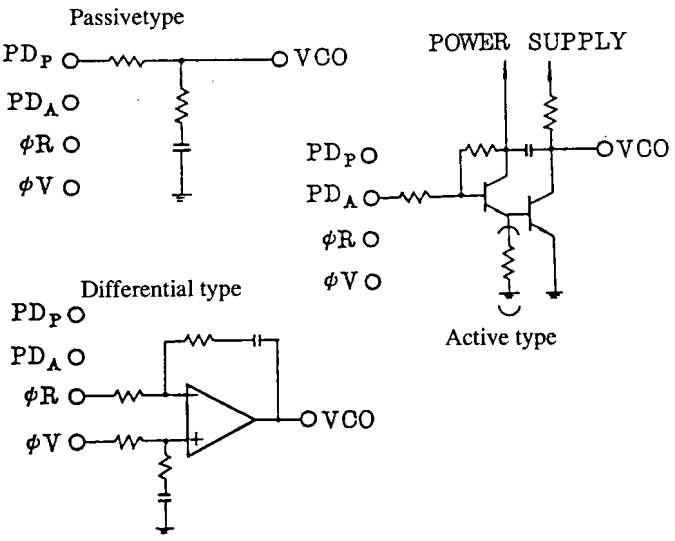
RA2	RA1	RA0	Divider ratio
0	0	0	16
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	3668
1	0	1	4096
1	1	0	6144
1	1	1	8192

NAME (No.)	DESCRIPTION
CLOCK (10) DATA (11)	Shift register data and clock input. Data shifts by 1 bit when CLOCK changes from "L" to "H". The shift register configuration is shown below. Make the input data format coincide with the shift register configuration. 
ENABLE (12)	Latch write signal. When "H", writing is enabled. Internal pull-up resistor.
TEST (14)	Test pin. Should be left open during normal operation. Internal pull-down resistor.
REFOUT (15)	Buffered reference oscillator (XIN, XOUT) output. Recommend to connect a load to this pin for stable oscillation.
XOUT (16) XIN (17)	Pin for a quartz crystal oscillator. Internal feedback resistor is provided for AC coupling. Input an external clock to the XIN pin via a capacitor.

■ PHASE DETECTOR TIMING CHART

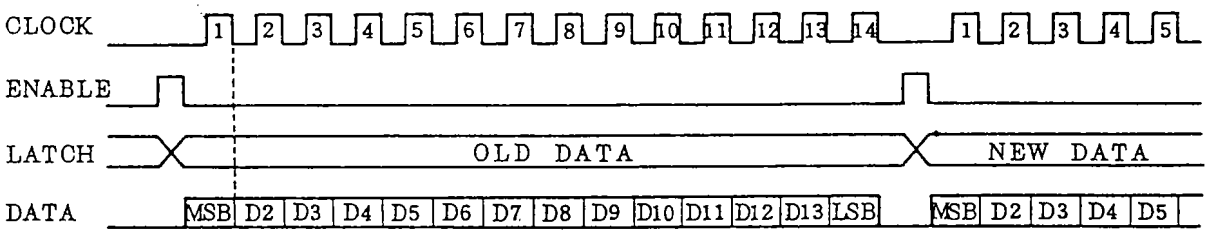


■ LOWPASS FILTER

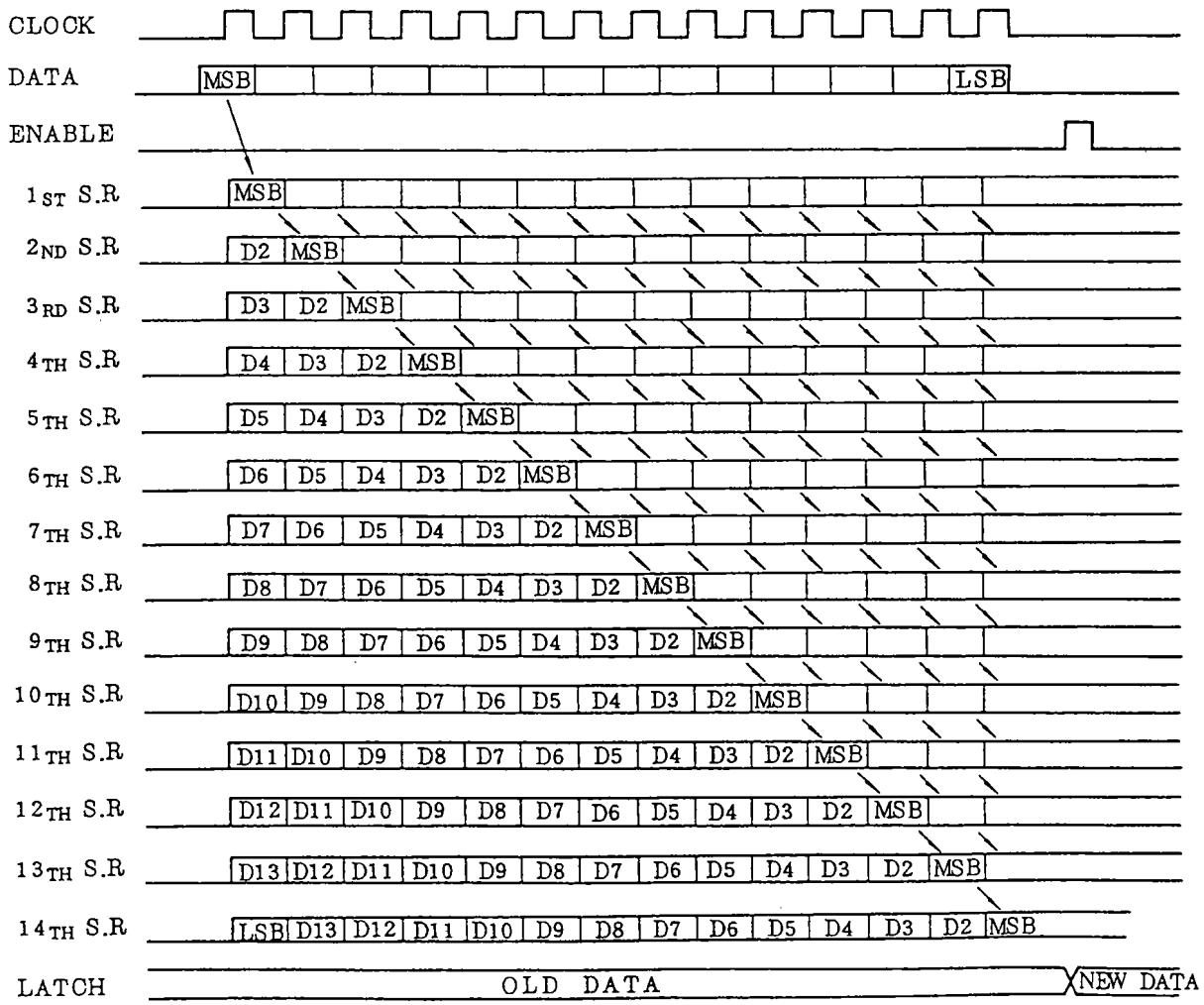


■ TIMING CHART

● Input frequency divider data setting



- Input data MSB first.
- Data is input on the rising edge of CLOCK, so it is necessary to change data on the falling edge of CLOCK.
- While the ENABLE signal is "H", data is transferred from the shift register to the input frequency divider's latch. Therefore, ENABLE must go "L" while data is being written into the shift register.



■ ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply voltage	V_{DD}-V_{SS}	-0.3 to +7.0	V
Input voltage	V_{IN}	V_{SS}-30 toV_{DD}+0.3	V
Operating temperature	T_{OPR}	-30 to +80	°C
Storage temperature	T_{STG}	-40 to +125	°C
Soldering temperature	T_{SLD}	260±5	°C
Soldering time	t_{SLD}	10	Sec

Setup time, hold time

■ ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, Ta = -30 to +80 °C

ITEM		SYMBOL	CONDITIONS	LIMITS			UNIT	REMARKS
				MIN	TYP	MAX		
Supply voltage		V_{DD}		4.5		5.5	V	
Current consumption		I_{DD}	F_{IN}=sine wave 30MHz 500mV_{p-p} X_{IN}=sine wave 15MHz 1V_{p-p}		4.0	8.0	mA	* Output pin open
Maximum operating frequency 1		F_{MAX1}	F_{IN}=sine wave 500mV_{p-p}	30	50		MHz	F_{IN}
Maximum operating frequency 2		F_{MAX2}	X_{IN}=sine wave 1V_{p-p}	15	50		MHz	X_{IN}
Input voltage		V_{INAC}	F_{IN}=AC coupling	0.5		V_{DD}-0.5	V	F_{IN}
			X_{IN}=AC coupling	1.0		V_{DD}-0.5		X_{IN}
Input voltage		V_{IH}		V_{DD}-0.3		V_{DD}	V	RA0 to RA2DAT, CLK, LE
		V_{IL}		0		0.5		
Input current 1		I_{IH1}	V_{IH1}=V_{DD}			15	µA	F_{IN}, X_{IN}
		I_{IL1}	V_{IL1}=0V			15		
Input current 2		I_{IL2}	V_{IL2}=0V			30	µA	ENABLE
Input current 3		I_{IH3}	V_{IH3}=V_{DD} Ta=25°C		0.001	0.1	µA	RA0 to RA2 DAT, CLK
		I_{IL3}	V_{IL3}=0V Ta=25°C		0.001	0.1		
Output current PDA, REFOUT		I_{OH}	V_{OH}=V_{DD}-0.4V	0.4			µA	øV, øR, PDP PDA, REFOUT
		I_{OL}	V_{OL}=0.4V	0.4				
Output leak current		I_{LH}	V_{LH}=V_{DD} Ta=25°C		0.001	0.1	µA	PDP
		I_{LL}	V_{LL}=0V Ta=25°C		0.001	0.1		PDA
Setup time	DAT → CLK	t_{SU1}		300			ns	Fig. 1
	CLK → LE	t_{SU2}		300				
Hold time	CLK → DAT	t_H		300			ns	