

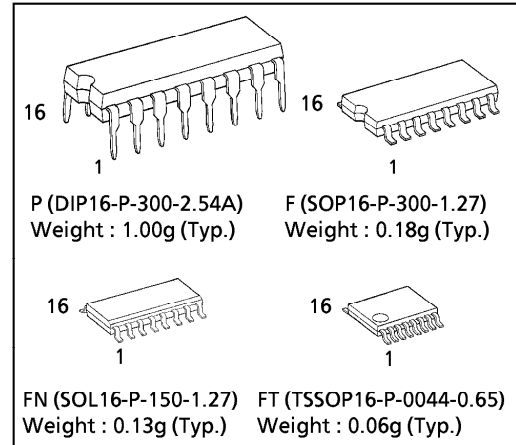
### TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC4051BP, TC4051BF, TC4051BFN, TC4051BFT**  
**TC4052BP, TC4052BF, TC4052BFN, TC4052BFT**  
**TC4053BP, TC4053BF, TC4053BFN, TC4053BFT**

**TC4051B SINGLE 8-CHANNEL MULTIPLEXER / DEMULTIPLEXER**  
**TC4052B DIFFERENTIAL 4-CHANNEL MULTIPLEXER / DEMULTIPLEXER**  
**TC4053B TRIPLE 2-CHANNEL MULTIPLEXER / DEMULTIPLEXER**

(Note) The JEDEC SOP (FN) is not available in Japan.

TC4051B, TC4052B and TC4053B are multiplexers with capabilities of selection and mixture of analog signal and digital signal. TC4051B has 8 channels configuration. TC4052B has 4 channel×2 configuration and TC4053B has 2 channel×3 configuration. The digital signal to the control terminal turns "ON" the corresponding switch of each channel, with large amplitude ( $V_{DD}-V_{EE}$ ) can be switched by the control signal with small logical amplitude ( $V_{DD}-V_{SS}$ ). For example, in the case of  $V_{DD}=5V$   $V_{SS}=0V$  and  $V_{EE}=-5V$ , signals between  $-5V$  and  $+5V$  can be switched from the logical circuit with single power supply of 5 volts. As the ON-resistance of each switch is low, these can be connected to the circuits with low input impedance.



#### MAXIMUM RATINGS

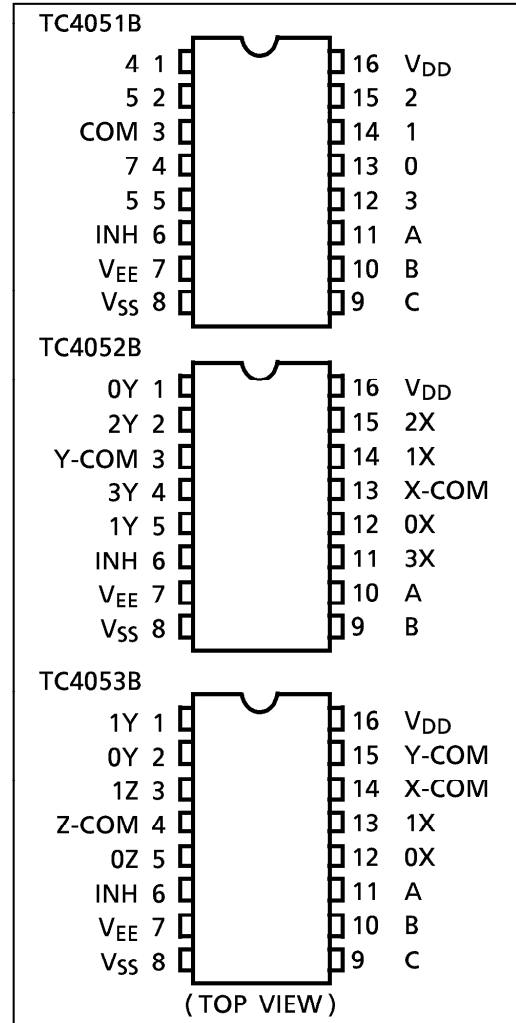
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	$V_{DD}-V_{SS}$	-0.5~20	V
DC Supply Voltage	$V_{DD}-V_{EE}$	-0.5~20	V
Control Input Voltage	$V_{CIN}$	$V_{SS}-0.5\sim V_{DD}+0.5$	V
Switch I/O Voltage	$V_I/V_O$	$V_{EE}-0.5\sim V_{DD}+0.5$	V
Control Input Current	$I_{CIN}$	±10	mA
Potential difference across I/O during ON	$V_I-V_O$	-0.5~0.5	V
Power Dissipation	$P_D$	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	$T_{opr}$	-40~85	°C
Storage Temperature Range	$T_{stg}$	-65~150	°C

#### TRUTH TABLE

CONTROL INPUTS				"ON" CHANNEL		
INHIBIT	C△	B	A	TC4051B	TC4052B	TC4053B
L	L	L	L	0	0X, 0Y	0X, 0Y, 0Z
L	L	L	H	1	1X, 1Y	1X, 0Y, 0Z
L	L	H	L	2	2X, 2Y	0X, 1Y, 0Z
L	L	H	H	3	3X, 3Y	1X, 1Y, 0Z
L	H	L	L	4	—	0X, 0Y, 1Z
L	H	L	H	5	—	1X, 0Y, 1Z
L	H	H	L	6	—	0X, 1Y, 1Z
L	H	H	H	7	—	1X, 1Y, 1Z
H	*	*	*	NONE	NONE	NONE

\* : Don't Care    △ Except TC4052B

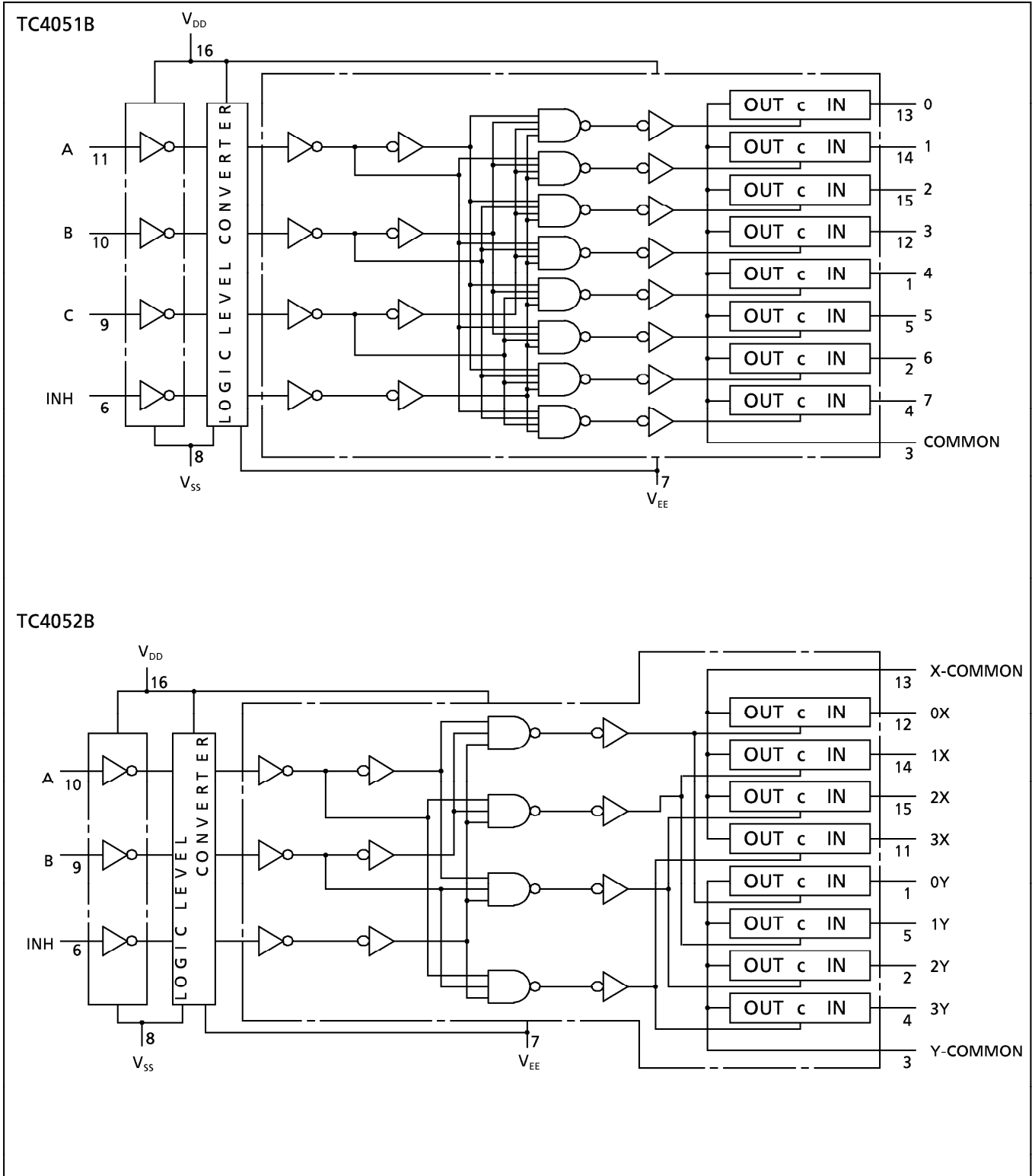
#### PIN ASSIGNMENT



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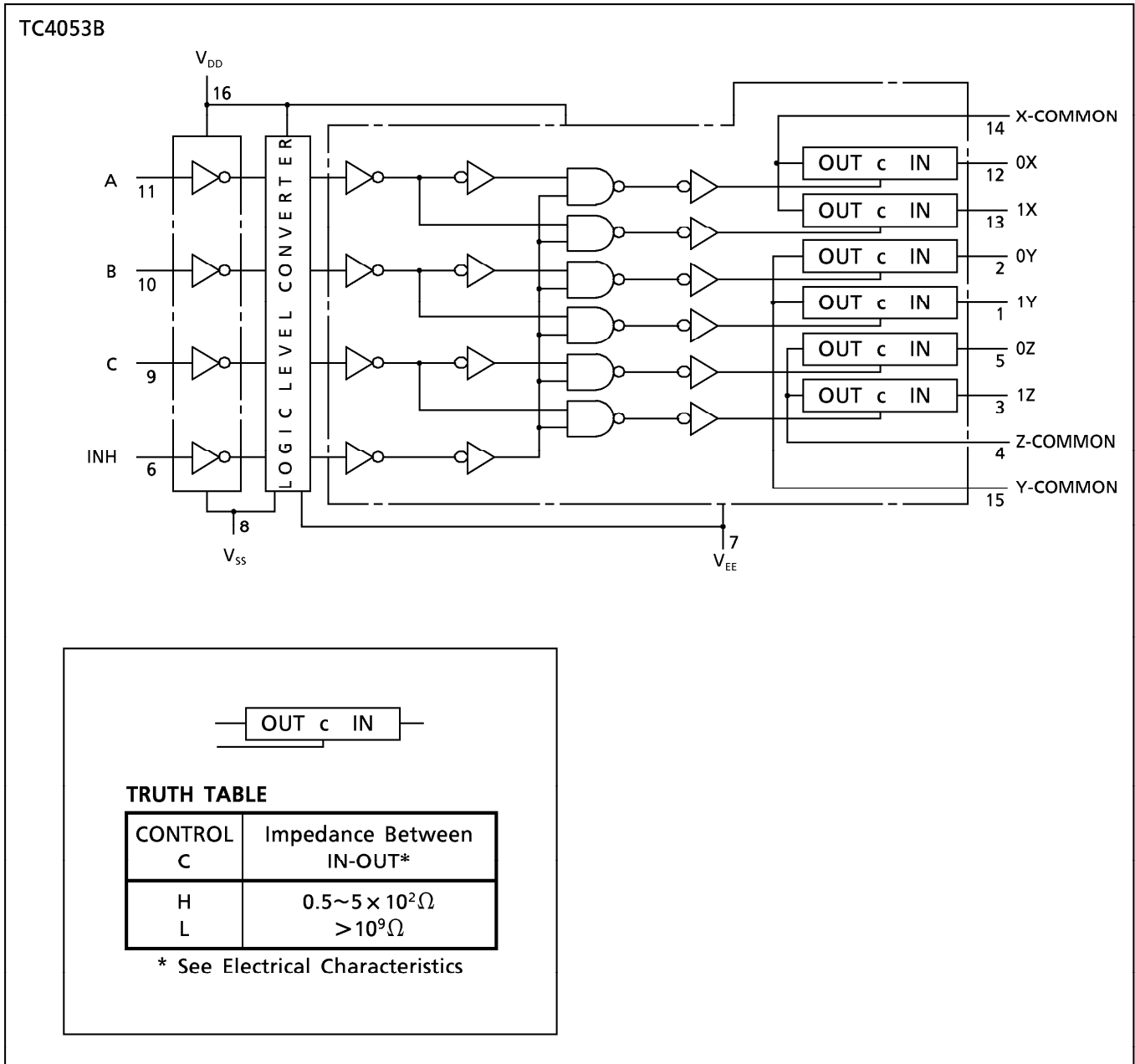
**LOGIC DIAGRAM**



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- The information contained herein is subject to change without notice.

**LOGIC DIAGRAM**



**RECOMMENDED OPERATING CONDITIONS**

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	$V_{DD}-V_{SS}$		3	—	18	V
	$V_{DD}-V_{EE}$		3	—	18	
Control Input Voltage	$V_{IN}$		$V_{SS}$	—	$V_{DD}$	V
Input/Output Voltage	$V_{IN}/V_{OUT}$		$V_{EE}$	—	$V_{DD}$	V

**STATIC ELECTRICAL CHARACTERISTICS**

CHARACTERISTIC	SYM-BOL	TEST CONDI-TION	V <sub>SS</sub> (V)			- 40°C		25°C			85°C		UNIT
			V <sub>EE</sub> (V)	V <sub>DD</sub> (V)	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
Control Input High Voltage	$V_{IH}$	$V_{IS} = V_{DD}$ thru 1k $\Omega$	$V_{EE} = V_{SS}$	5	3.5	—	3.5	2.75	—	3.5	—	V	
			$R_L = 1k\Omega$	10	7.0	—	7.0	5.50	—	7.0	—		
			to $V_{SS}$	15	11.0	—	11.0	8.25	—	11.0	—		
Control Input Low Voltage	$V_{IL}$		$I_{IS} < 2\mu A$	5	—	1.5	—	2.25	1.5	—	1.5	V	
			on all OFF channels	10	—	3.0	—	4.5	3.0	—	3.0		
				15	—	4.0	—	6.75	4.0	—	4.0		
On-State Resistance	$R_{ON}$	$0 \leq V_{IS} \leq V_{DD}$ $R_L = 10k\Omega$	0	0	5	—	850	—	240	950	—	1200	$\Omega$
			0	0	10	—	210	—	110	250	—	300	
			0	0	15	—	140	—	80	160	—	200	
$\Delta$ On-State Resistance Between Any 2 Switches	$R_{ON\Delta}$		0	0	5	—	—	—	10	—	—	—	$\Omega$
			0	0	10	—	—	—	6	—	—	—	
			0	0	15	—	—	—	4	—	—	—	
Input/Output Leakage Current	$I_{OFF}$	$V_{IN} = 18V, V_{OUT} = 0V$ $V_{IN} = 0V, V_{OUT} = 18V$		18	—	$\pm 100$	—	$\pm 0.01$	$\pm 100$	—	$\pm 1000$	nA	
				18	—	$\pm 100$	—	$\pm 0.01$	$\pm 100$	—	$\pm 1000$		
Quiescent Supply Current	$I_{DD}$	$V_{IN} = V_{SS}, V_{DD}^*$		5	—	5.0	—	0.005	5.0	—	150	$\mu A$	
				10	—	10	—	0.010	10	—	300		
				15	—	20	—	0.015	20	—	600		
Input Current	$I_{IN}$	$V_{IH} = 18V$ $V_{IL} = 0V$		18	—	0.1	—	$10^{-5}$	0.1	—	1.0	$\mu A$	
				18	—	-0.1	—	$-10^{-5}$	-0.1	—	-1.0		
Input Capacitance	$C_{IN}$				—	—	—	5	7.5	—	—	pF	
Switch Input Capacitance	$C_{IN}$				—	—	—	10	—	—	—		
Output Capacitance	$C_{OUT}$	TC4051B TC4052B TC4053B		10	—	—	—	58	—	—	—		pF
				10	—	—	—	30	—	—	—		
				10	—	—	—	17	—	—	—		
Feedthrough Capacitance	$C_{IN-}$ $C_{OUT}$	TC4051B TC4052B TC4053B		10	—	—	—	0.2	—	—	—	pF	
				10	—	—	—	0.2	—	—	—		
				10	—	—	—	0.2	—	—	—		

\* All valid input combinations.

**DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, CL = 50pF)**

CHARACTERISTIC	SYMBOL	TEST CONDITION	V <sub>DD</sub> (V)			MIN.	TYP.	MAX.	UNIT
			V <sub>SS</sub> (V)	V <sub>EE</sub> (V)	V <sub>DD</sub> (V)				
Phase Difference Between Input to Output	φ <sub>I</sub> - O		0	0	5	—	15	45	ns
			0	0	10	—	8	20	
			0	0	15	—	6	15	
Propagation Delay Time (A, B, C, - OUT)	t <sub>pZL</sub> t <sub>pZH</sub> t <sub>pLZ</sub> t <sub>pHZ</sub>	R <sub>L</sub> = 1kΩ	0	0	5	—	170	550	
			0	0	10	—	90	240	
			0	0	15	—	70	160	
			0	-5	5	—	100	240	
			0	-7.5	7.5	—	80	160	
Propagation Delay Time (INH - OUT)	t <sub>pZL</sub> t <sub>pZH</sub>	R <sub>L</sub> = 1kΩ	0	0	5	—	120	380	
			0	0	10	—	60	200	
			0	0	15	—	50	160	
			0	-5	5	—	80	200	
			0	-7.5	7.5	—	60	160	
Propagation Delay Time (INH - OUT)	t <sub>pLZ</sub> t <sub>pHZ</sub>	R <sub>L</sub> = 1kΩ	0	0	5	—	170	450	
			0	0	10	—	90	210	
			0	0	15	—	70	160	
			0	-5	5	—	100	210	
			0	-7.5	7.5	—	80	160	
- 3dB Cutoff Frequency TC4051B TC4052B TC4053B	f <sub>MAX</sub> (I - O)	R <sub>L</sub> = 1kΩ (*1)	-5	-5	5	—	20	—	MHz
			-5	-5	5	—	30	—	
			-5	-5	5	—	40	—	
Total Harmonic Distortion	—	R <sub>L</sub> = 10kΩ f = 1kHz (*2)	-2.5	-2.5	2.5	—	0.15	—	%
			-5	-5	5	—	0.03	—	
			-7.5	-7.5	7.5	—	0.02	—	
- 50dB Feedthrough (SWITCH OFF)	—	R <sub>L</sub> = 1kΩ (*3)	-5	-5	5	—	500	—	kHz
Crosstalk	—	R <sub>L</sub> = 1kΩ (*4)	-5	-5	5	—	1.5	—	MHz
Crosstalk (CONTROL - OUT)	—	R <sub>IN</sub> = 1kΩ R <sub>OUT</sub> = 10kΩ C <sub>L</sub> = 15pF	0	0	5	—	200	—	mV
			0	0	10	—	400	—	
			0	0	15	—	600	—	

\*1 Sine wave of ±2.5Vp-p shall be used for V<sub>is</sub> and the frequency of 20 log 10  $\frac{V_{OS}}{V_{is}}$  = -3dB shall be f<sub>MAX</sub>.

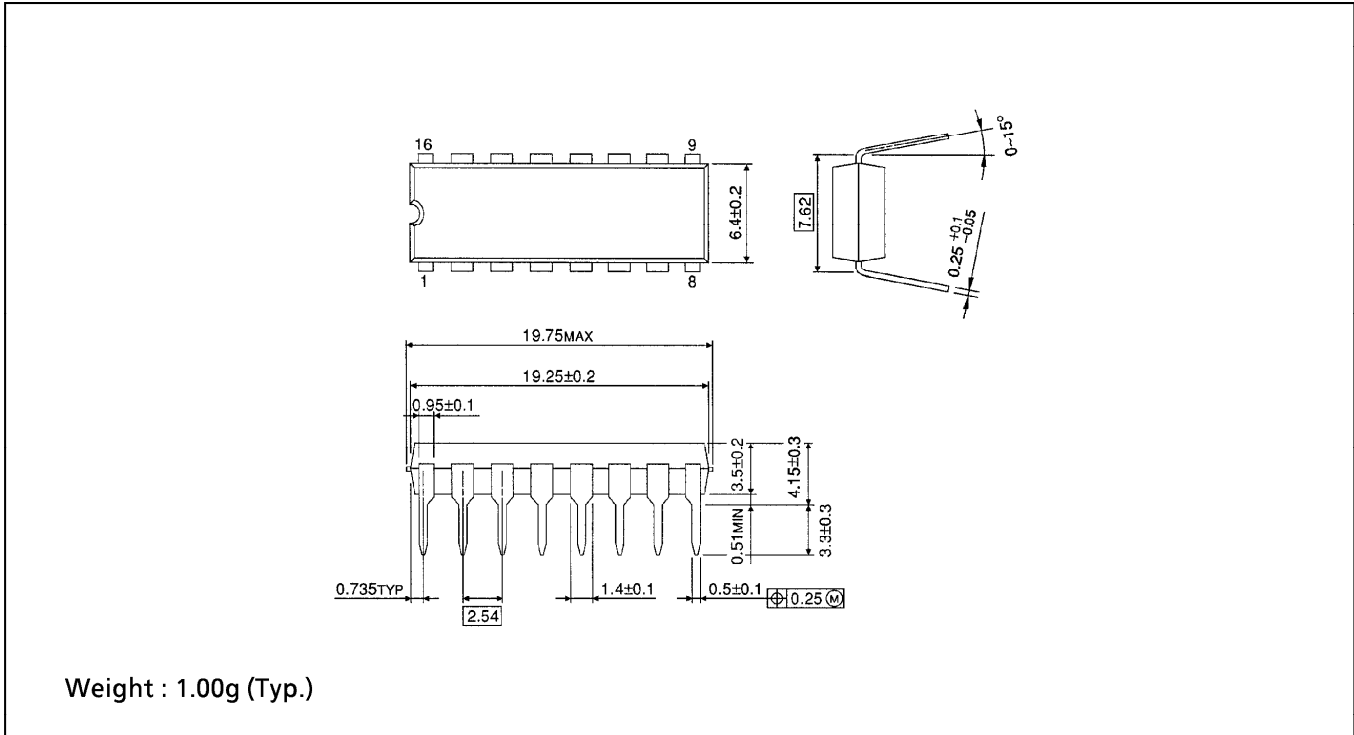
\*2 V<sub>is</sub> shall be sine wave of ±  $\left(\frac{V_{DD}-V_{EE}}{4}\right)$  p-p.

\*3 Sine wave of ±2.5Vp-p shall be used for V<sub>is</sub> and the frequency of 20 log 10  $\frac{V_{OS}}{V_{is}}$  = -50dB shall be feed-through.

\*4 Sine wave of ±2.5Vp-p shall be used for V<sub>is</sub> and the frequency of 20 log 10  $\frac{V_{OS}}{V_{is}}$  = -50dB shall be Crosstalk.

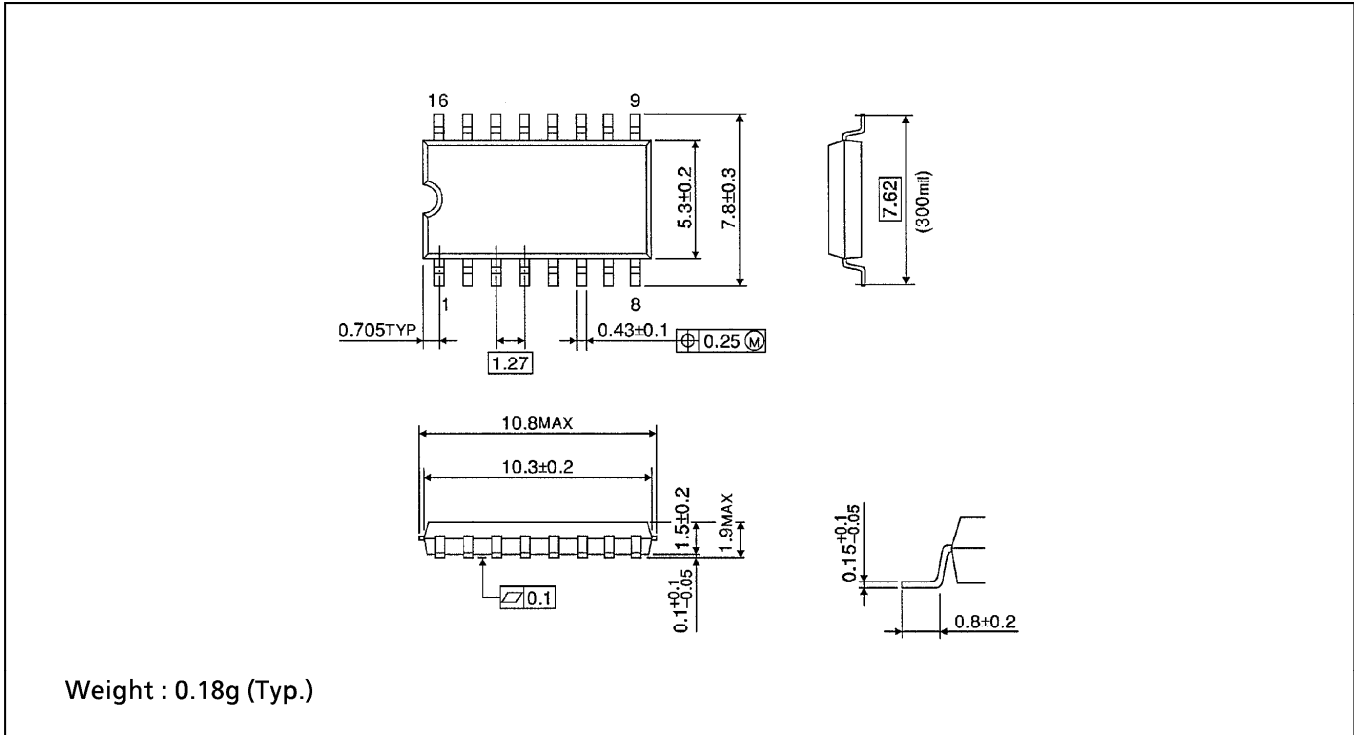
**DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)**

Unit in mm



**SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)**

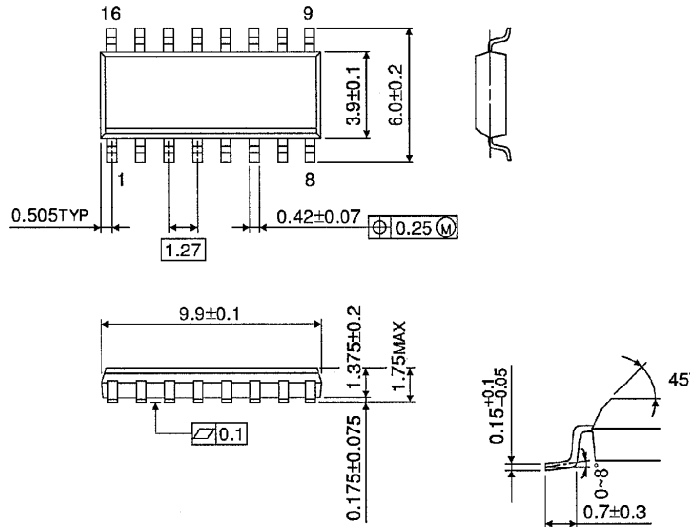
Unit in mm



**SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150-1.27)**

Unit in mm

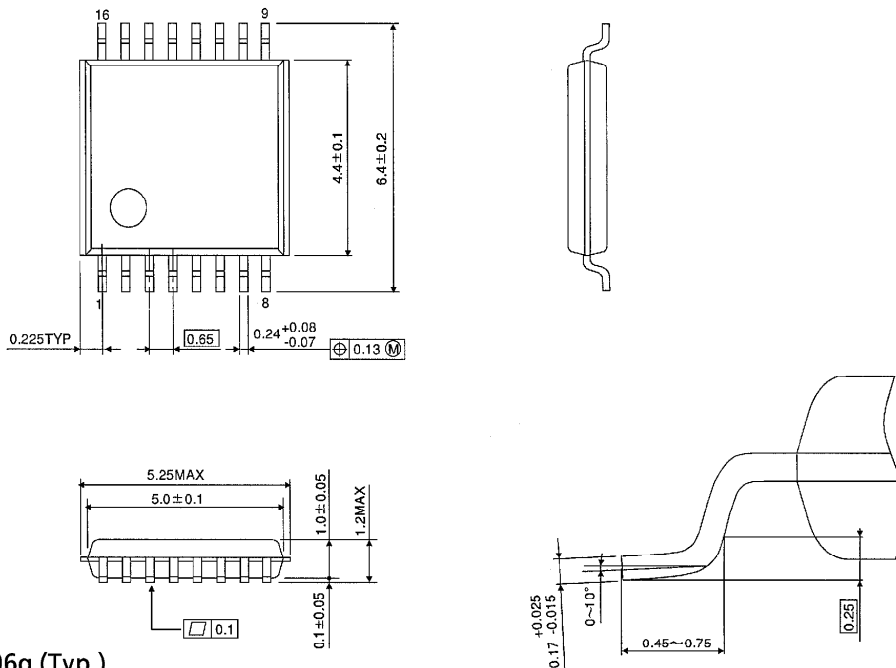
(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

**TSSOP 16PIN OUTLINE DRAWING (TSSOP16-P-0044-0.65)**

Unit in mm



Weight : 0.06g (Typ.)