

TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

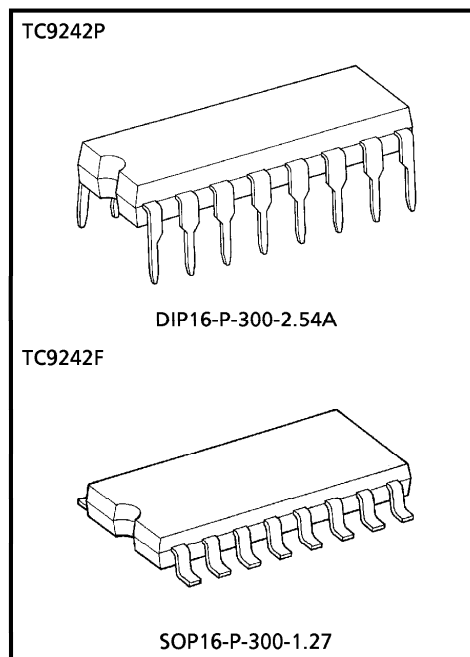
# TC9242P, TC9242F

## QUARTZ PLL MOTOR CONTROL

The TC9242P, TC9242F are CMOS LSIs developed for controlling the motor speed. Since an 8bit D/A converter system has been employed for each of the speed control system (AFC) and the phase control system (APC). Offers improved linearity. With frequency division ratios of 1/3, 1/4 and 1/5 the standard divider is ideal for laser scanner motors.

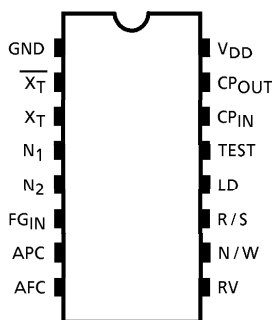
### FEATURES

- Crystal can be used up to 20MHz, and crystal reference dividing frequency is selectable from three positions of 1/3, 1/4 and 1/5.
- Lock range can be selected from two positions of 1/20 and 1/27.
- External oscillator makes possible fine adjustment of speed.
- Lock detection output and reverse rotation signal output are provided.
- Package is DIP16PIN and SOP16PIN.



Weight  
 DIP16-P-300-2.54A : 1.00g (Typ.)  
 SOP16-P-300-1.27 : 0.16g (Typ.)

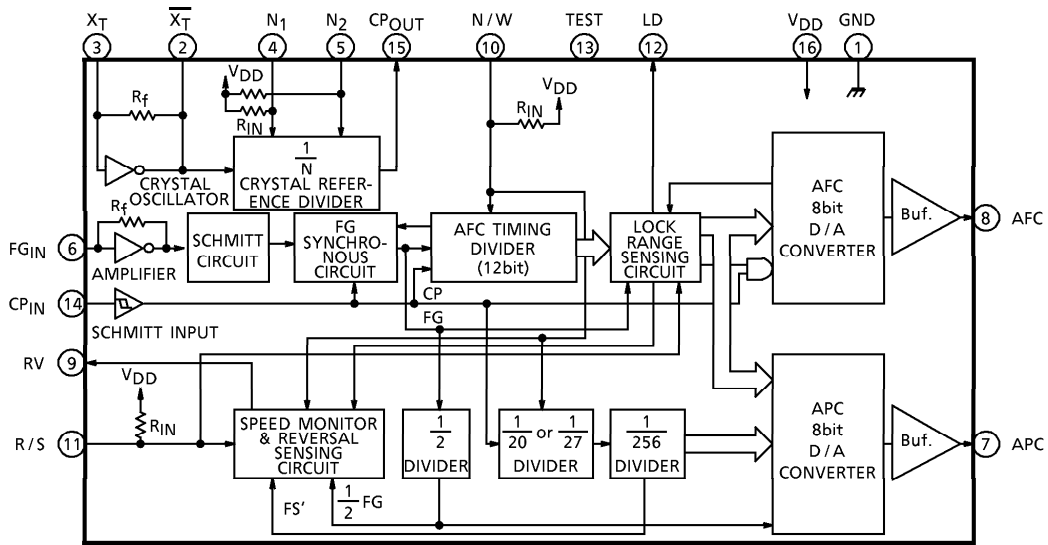
### PIN CONNECTIONS (TOP VIEW)



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**BLOCK DIAGRAM**



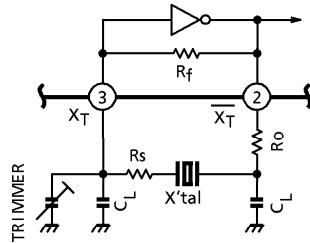
**FUNCTIONAL EXPLANATION OF EACH TERMINAL**

PIN No.	SYMBOL	PIN NAME	FUNCTIONAL & OPERATION EXPLANATION	REMARKS
16	V <sub>DD</sub>	Power Terminal	V <sub>DD</sub> = 5V ± 0.5V is applied.	—
1	GND	Ground Terminal	Ground	—
2	X <sub>T</sub>	Crystal Oscillation Terminal	Crystal oscillator is connected.	With a built-in feedback resistor.
3	X <sub>T</sub>			
4	N <sub>1</sub>	Reference Divided Frequency Switching Terminal	Switching of divided frequency from the crystal reference frequency divider into 1/3, 1/4 and 1/5 is possible.	With a built-in pull-up resistor.
5	N <sub>2</sub>			
6	FG <sub>IN</sub>	FG Pulse Input Terminal	Input terminal for pulse showing motor speed.	With a built-in amplifier.
7	APC	APC Output Terminal	Output terminal for motor phase control system. Output of 8bit D/A converter.	With a built-in buffer.
8	AFC	AFC Output Terminal	Output terminal for motor speed control system. Output of 8bit D/A converter.	With a built-in buffer.
9	RV	Reverse Signal Output Terminal	Terminal for motor reverse signal output.	CMOS OUTPUT
10	N/W	Lock range Switching Terminal	Terminal for switching motor speed. L = 1/27, H or NC = 1/20.	With a built-in pull-up resistor.
11	R/S	RUN/STOP Input Terminal	Motor RUN/STOP signal input terminal L = RUN, H or NC = STOP	With a built-in pull-up resistor.
12	LD	Lock Detecting Terminal	This terminal becomes "H" when the motor speed is within the lock range and otherwise "L".	CMOS OUTPUT
14	CP <sub>IN</sub>	Reference Frequency Input Terminal	Normally connected to CPOUT. For external fine adjustment input from an external oscillator.	CMOS SCHMITT INPUT
15	CP <sub>OUT</sub>	Reference Frequency Output Terminal	Terminal for divided output from the crystal reference frequency divider. Normally connected to CP <sub>IN</sub> .	CMOS OUTPUT
13	TEST	Output Terminal for INTERNAL TEST	Output terminal for INTERNAL TEST. Generally open.	—

**EXPLANATION OF OPERATION**

1. Crystal Oscillation Terminals ( $X_T, \overline{X_T}$ )

- The crystal oscillator is used by connecting as shown below.



※ CL of 10~30pF is appropriate.

- Crystal oscillation frequency is calculated by the following equation according to number of FG pulses of a motor to be used.

$$f_X = \frac{R}{60} \times FG' \times 128 \times (20 \text{ or } 27) \times N \text{ (Hz)}$$

Note : (20 or 27) : 20 at N/W = "H" or NC  
27 at N/W = "L"

Further,  $f_X$  : Crystal oscillation frequency,  $FG'$  : No. of FG pulses generated per revolution of motor.

$N$  : Ratio of frequency division of the crystal reference frequency divider.  
 $N = 3, 4, 5$  (Refer to Item 9.)

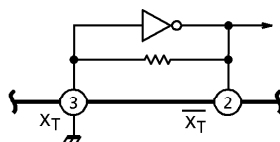
- Maximum operating frequency is above 20MHz and crystals up to 20MHz can be used.
- If necessary, adjust  $R_o$ ,  $R_s$  and  $C_L$  to control noise from the crystal oscillator circuit or to control overtone oscillation.

<Reference values>

$f_{XT}$ (MHz)	$R_o$ ( $\Omega$ )	$R_s$ ( $\Omega$ )	$C_L$ (pF)
20	—	220	22
12	—	220	27
8	—	220	30
4.5	2.2k	—	30
1.5	4.7k	—	30

Note : The values in the table are the reference values. Determine the values suitable for the characteristics of the crystal used.

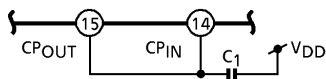
Note : When not using the crystal oscillator circuit, always connect pin 3 ( $X_T$ ) to GND as shown in the diagram to overcome the effects of noise and to reduce current consumption.



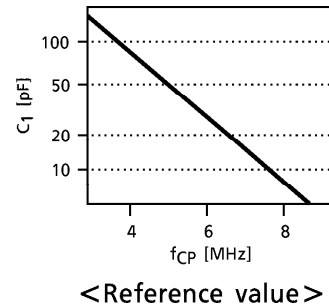
<When not using the crystal oscillator circuit>

2. Reference Frequency Input / Output Terminals (C<sub>POUT</sub>, C<sub>PIN</sub>)

- Divided output  $\frac{f_x}{N}$  from the crystal reference frequency divider is available at C<sub>POUT</sub>, which is normally connected to C<sub>PIN</sub>.
- When an external oscillator (CR oscillator, etc.) is connected to C<sub>PIN</sub>, motor speed can be finally adjusted.
- If the effects of noise from C<sub>PIN</sub> input signal overshoot must be controlled, connect capacitor C<sub>1</sub> as in the following diagram.

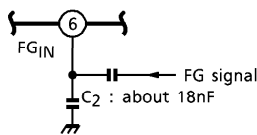


Note : When connecting capacitor C<sub>1</sub>, make sure that the input level of pin 14 (C<sub>PIN</sub>) does not fall below the standard ( $V_{IH} \geq 0.8 \times V_{DD}$ ,  $V_L \leq 0.2 \times V_{DD}$ )



3. FG Pulse Input Terminal (F<sub>G</sub>I<sub>N</sub>)

- This is the input terminal of FG pulse that shows the motor speed. This FG pulse becomes comparison frequency.
- This terminal has built-in Amplifier and Schmitt circuit. FG pulses are applied through capacitor coupling and small amplitude is enough for proper operation.
- If there is noise in the FG signal, connect capacitor C<sub>2</sub> as shown in the diagram to control the noise.



Note : Determine the values of capacitors C<sub>1</sub> and C<sub>2</sub> after checking their characteristics with f<sub>CP</sub> and f<sub>FG</sub> used.

Note : When connecting capacitor C<sub>2</sub>, make sure that the input level of pin 6 (F<sub>G</sub>I<sub>N</sub>) does not fall below the standard ( $V_{inFG} \geq 0.5V_{p-p}$ )

4. Lock Range Switching Terminal (N/W)

This terminal is for switching the Lock range with a pull-up resistor and chattering preventive circuit.

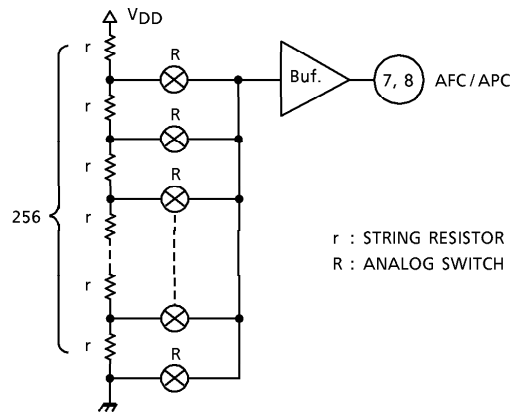
(TRUTH TABLE)

N / W	DIVIDED FREQUENCY	LOCK RANGE
L	$\frac{1}{27}$	+ 3.4 ~ - 3.9% of reference cycle
H or NC	$\frac{1}{20}$	+ 4.6 ~ - 5.3% of reference cycle

CAUTION reference frequency  $FS = f_x / N \times (20 \text{ or } 27) \times 128 \text{ (Hz)}$ ,  $FS' = \frac{FS}{2}$

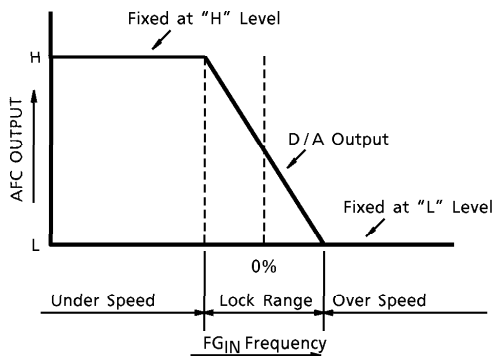
5. APC, AFC Output Terminal (APC, AFC)

- AFC (speed control output) is a F-V converter for FG frequency and is consisting of a 8bit D/A converter.
- APC (phase control output) is a phase comparator ( $\phi$ -V converter) that compares phase difference  $\phi$  between 1/2 FG and reference frequency  $FS'$ , and is also consisting of a 8bit D/A converter.

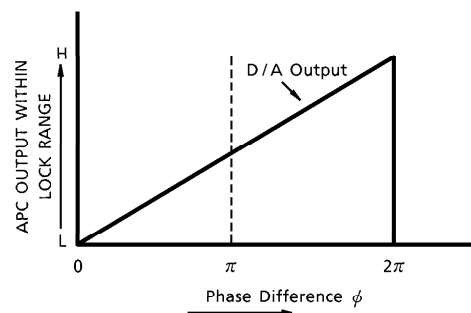


- Both APC and AFC perform the following 3 operations according to  $FG_{IN}$  frequency.
  - When  $FG_{IN}$  frequency is within the lock range:  
Both APC and AFC perform the normal operation for  $FG_{IN}$ .
  - When  $FG_{IN}$  frequency is below the lock range (under speed):  
APC and AFC outputs are both fixed at "H" level.
  - When  $FG_{IN}$  frequency is above the lock range (over speed):  
APC and AFC outputs are both fixed at "L" level.
- When a motor is in STOP state ( $P/S = H$  or  $NC$ ), both AFC and APC are fixed "L" level.

AFC output change status for  $FG_{IN}$  frequency

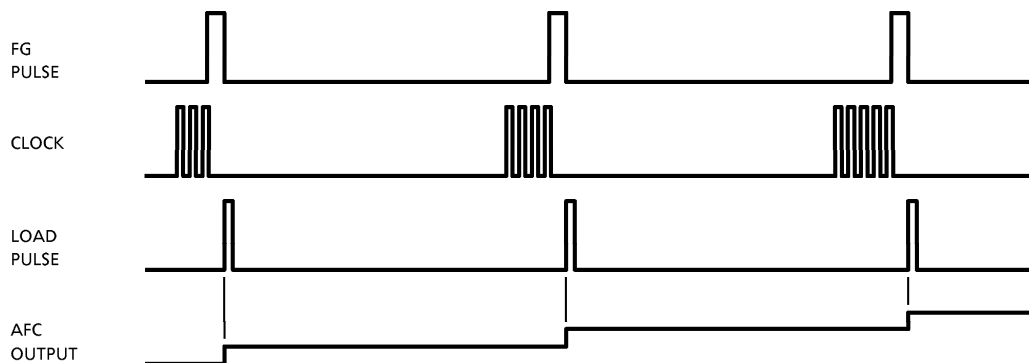


APC output change status for phase difference  $\phi$

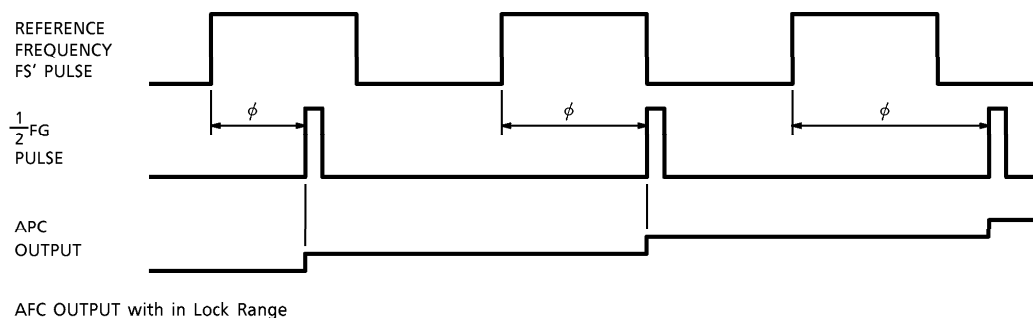


- AFC and APC timing chart within lock range.

a. AFC (SPEED CONTROL SYSTEM)



b. APC (PHASE CONTROL SYSTEM)



6. Lock Detecting Terminal (LD)

- This terminal is the lock detecting output and is placed at "H" level when  $FG_{IN}$  frequency is within the lock range and otherwise, placed at "L" level.

7. RUN/STOP Input Terminal (R/S)

- RUN/STOP signals of the motor are input to this terminal.  
PLAY = L, STOP = H or NC.
- This terminal has a pull-up resistor and a chattering preventive circuit.
- During RUN (R/S=L), AFC, APC and LD perform the above-mentioned operations for  $FG_{IN}$  frequency, and during STOP (R/S=H or NC), AFC, APC and LD are all fixed at "L" level.

8. Reverse Signal Output Terminal (RV)

- Reverse signal for braking the motor at time of switching of Lock range from 1/20 to 1/27 or the operation from RUN to STOP is output through this terminal.
- Change of RV output status

PREVIOUS STATUS	RV OUTPUT CHANGE TO "H" LEVEL	RV OUTPUT CHANGE TO "L" LEVEL
During Normal Rotation (During Lock) at 1/20	When the Lock range is switched from 1/20 to 1/27.	When the Lock range is locked at 1/27, or When $FG_{IN} \leq 1/8FS$ , or when the Lock range is switched from 1/27 to 1/20.
During Normal Rotation (During Lock) at 1/20 or 1/27	When the operation is switched from RUN to STOP.	When $FG_{IN} \leq 1/8FS$ or when the operation is switched from STOP to RUN.

- In other cases than above, RV output is not changed and fixed at "L" level.
- Further, if FG frequency rises up to 1.5 times of normal rotation at 1/20 (2 times of normal rotation at 1/27), RV output is reset.

9. Reference Divided Frequency Switching Terminal (N<sub>1</sub>, N<sub>2</sub>)

- Divided frequency 1/N of the crystal reference frequency divider can be switched to 1/5, 1/4 or 1/3 by number of FG pulses or a crystal used.
- This terminal has a built-in pull-up resistor.

(TRUTH TABLE)

N1	N2	1/N
H	H	1/5
L	H	1/4
H	L	1/3

1/N : Crystal reference divided frequency

Note : Do not use N1 = N2 = L, which is used for internal test only.

## MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	-0.3~7.0	V
Input Voltage	V <sub>IN</sub>	-0.3~V <sub>DD</sub> + 0.3	V
Power Dissipation	P <sub>D</sub>	300	mW
Operating Temperature	T <sub>opr</sub>	-40~85	°C
Storage Temperature	T <sub>stg</sub>	-65~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified Ta = 25°C, V<sub>DD</sub> = 5V)

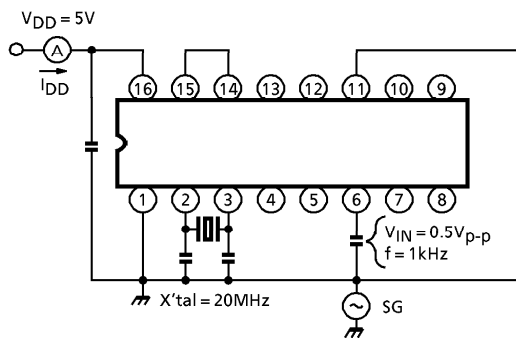
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		V <sub>DD</sub>	—	※	4.5	5.0	5.5	V
Operating Supply Current		I <sub>DD</sub>	1	X'tal = 20MHz, CP <sub>in</sub> = CP <sub>out</sub>	—	15.0	25.0	mA
Operating Frequency Range	X <sub>T</sub>	f <sub>XT</sub>	2	※	1.5	~	20.0	MHz
	CP <sub>in</sub>	f <sub>CP</sub>	3	V <sub>in</sub> Square Wave ※	0.3	~	10.0	MHz
	FG <sub>in</sub>	f <sub>FG</sub>	—	V <sub>in</sub> = 0.5V <sub>p-p</sub> Sine Wave ※	—	~	4.0	kHz
Input Amplitude Voltage	FG <sub>in</sub>	V <sub>inFG</sub>	4	f <sub>FG</sub> = 4kHz, Sine Wave, AC input ※	0.5	~	V <sub>DD</sub> - 0.5	V <sub>p-p</sub>
AFC, APC D/A Converter	Deviation	—	—	—	—	±2.0	±4.0	LSB
	Resolution	—	—	—	—	V <sub>DD</sub> /256	—	V
Pull-up Resistor		R <sub>in</sub>	—	N1, N2, N/W, R/S	15	30	60	kΩ
Input Voltage	"H" Level	V <sub>IH</sub>	—	N1, N2, N/W, R/S, CP <sub>in</sub>	V <sub>DD</sub> × 0.8	~	V <sub>DD</sub>	V
	"L" Level	V <sub>IL</sub>	—	N1, N2, N/W, R/S, CP <sub>in</sub>	0	~	V <sub>DD</sub> × 0.2	
Input Leak Current		I <sub>IH</sub>	—	CP <sub>in</sub>	—	—	±1.0	μA
		I <sub>IL</sub>	—	CP <sub>in</sub>				
Output Current	"H" Level	I <sub>OH</sub>	—	RV, LD, CP <sub>out</sub> V <sub>OH</sub> = 4.5V	-0.5	-2.5	—	mA
	"L" Level	I <sub>OL</sub>	—	RV, LD, CP <sub>out</sub> V <sub>OL</sub> = 0.5V	0.5	2.5	—	
	"H" Level	I <sub>OH</sub>	—	APC, AFC V <sub>OH</sub> = 4.5V	-0.3	-1.0	—	μA
	"L" Level	I <sub>OL</sub>	—	APC, AFC V <sub>OL</sub> = 0.5V	25	75	—	
Amplifier Feedback Resistor	X <sub>T</sub>	R <sub>f</sub>	5	—	150	330	660	kΩ
	FG <sub>in</sub>	R <sub>f</sub>	5	—	150	330	660	kΩ

※ : Guaranteed within the range of V<sub>DD</sub> = 4.5~5.5V, Ta = -40~85°C

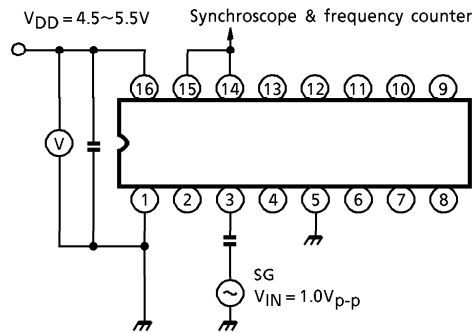


**TEST CIRCUIT**

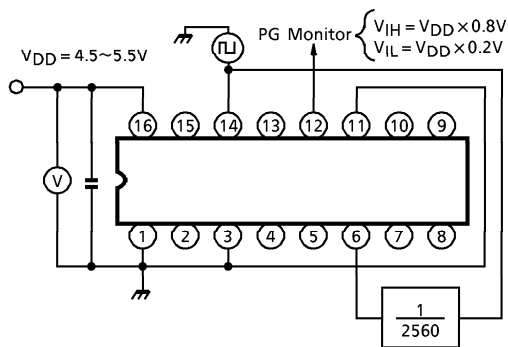
**1. Operating Supply Current  $I_{DD}$**



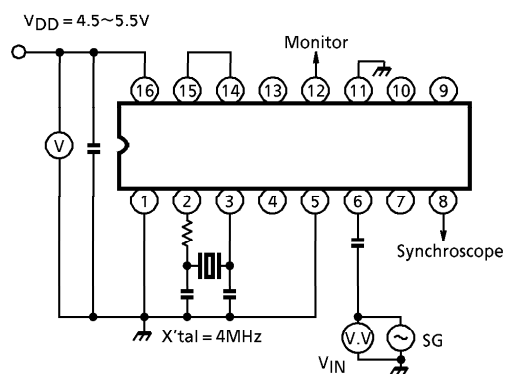
**2.  $X_T$  Operating Frequency Range  $f_{MAX}$  ( $f_{XT}$ )**



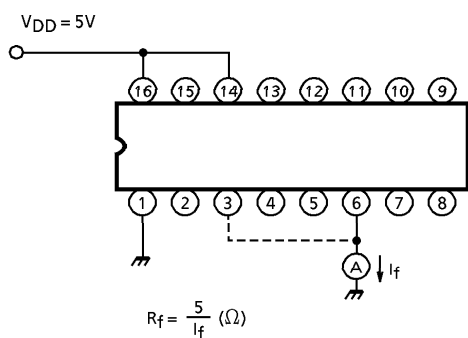
**3.  $CP_{IN}$  Operating Frequency Range  $f_{MAX}$  ( $f_{CP}$ )**



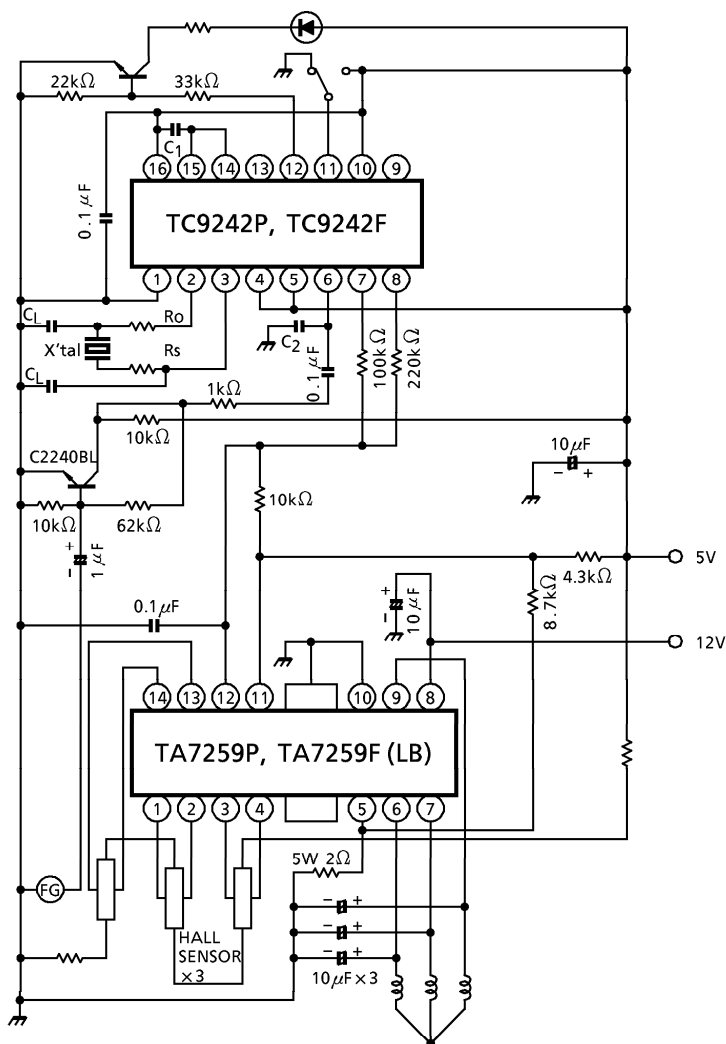
**4.  $FG_{IN}$  Input Sensitivity  $V_{INFG}$**



**5. Amplifier Feedback Resistor  $R_f$**



APPLICATION CIRCUIT



- Example of crystal oscillation frequency calculation.

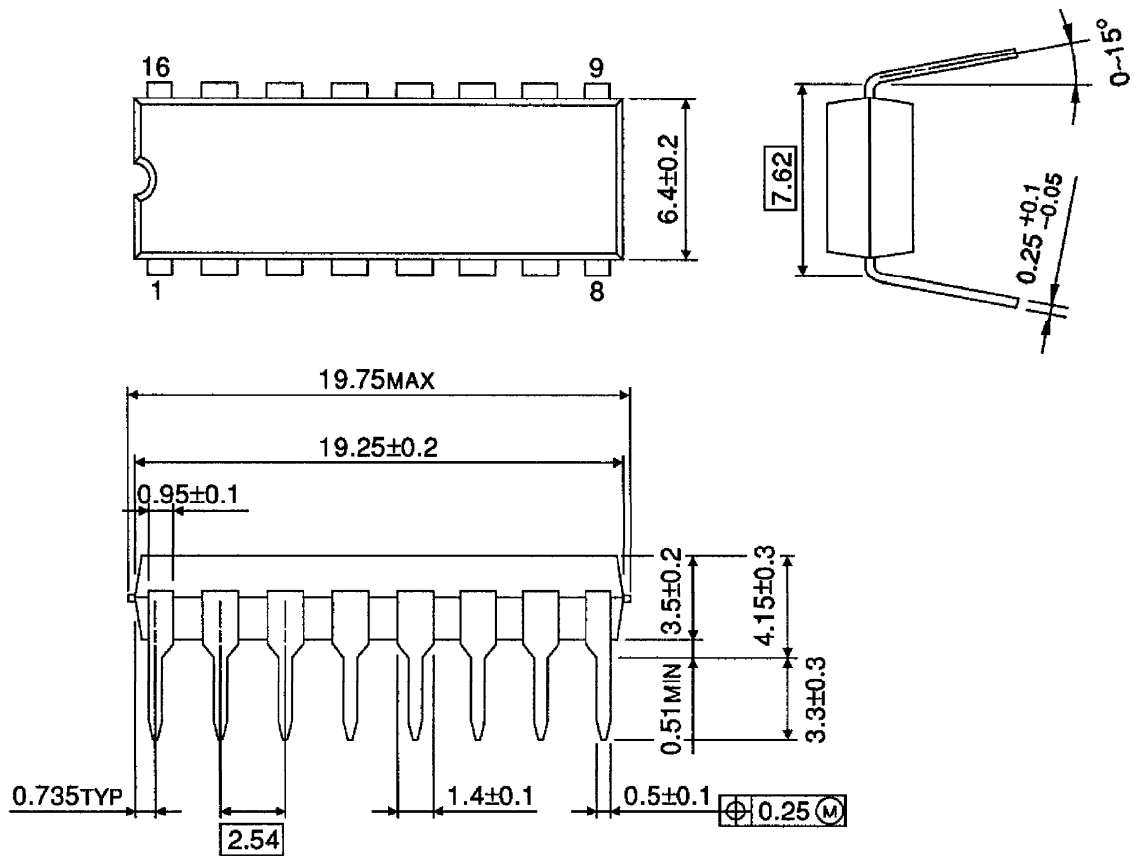
When FG' (number of FG pulse) = 180 pulses and R (revolution of motor) = 200rpm., if the dividing frequency of reference divider and lock range is set at N = 5 dividing frequency and N/W = 20, the crystal oscillation frequency  $f_x$  is as follows :

$$f_x = \frac{R}{60} \times FG' \times 128 \times 20 \times N = \frac{200}{60} \times 180 \times 128 \times 20 \times 5 = 7.68\text{MHz}$$

- Select the external filter of the differential amplifier in the application circuit depending on the response characteristics of the motor used.
- Determine values C1, C2, CL, Ro and Rs in the application circuit depending on the characteristics of the circuit.

**OUTLINE DRAWING**  
DIP16-P-300-2.54A

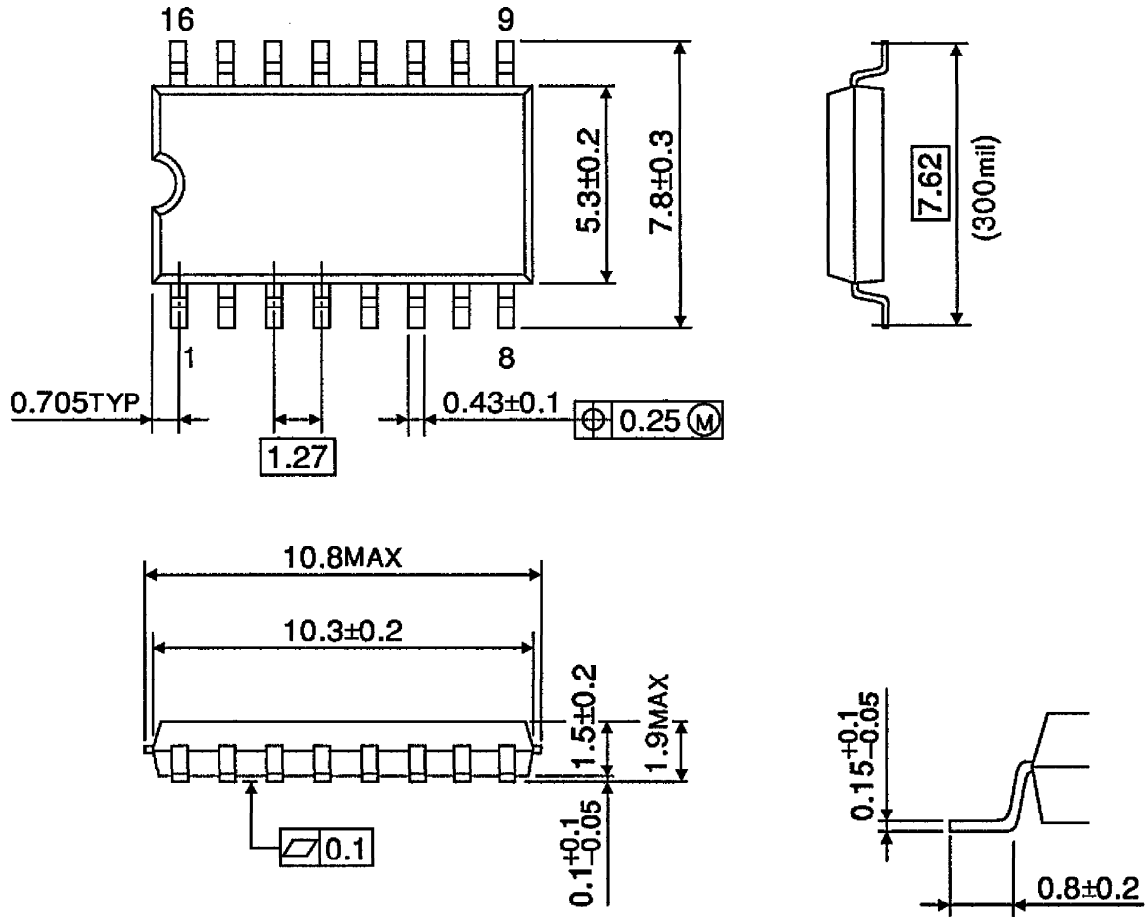
Unit : mm



Weight : 1.00g (Typ.)

**OUTLINE DRAWING**  
SOP16-P-300-1.27

Unit : mm



Weight : 0.16g (Typ.)